COE 360, Principles of VLSI Design, Term 043
Course Project

Modular Up-Down Counter

It is required to design a **3-bit Modular Up-Down Counter** circuit using CMOS technology. The Modular Up-Down Counter is to be designed as a generic one-bit Up-Down Counter cell that can be used to construct an n-bit counter by connecting n-cells. It is assumed that the counter has a **synchronous rising-edge clock**, **CLK**, and **asynchronous** reset, **RESET**. When RESET=1, the counter is reset to 0 asynchronously. The counter also has an **ENABLE** signal such that if ENABLE=1, the counter will be counting up or down. Otherwise the counter will remain in its current state. The direction of counting is controlled by the signal **DIR**. If DIR=0, the counter will be counting up otherwise it will be counting down.

To complete the project, you need to do the following step:

1. Derive the logic-level implementation of one-bit modular Up-Down Counter Cell. Verify by simulation the correct operation of the cell.

2. Using the one-bit Up-Down Counter Cell in 1, construct a 3-bit Up-Down Counter. Verify its correct operation in counting up and down across the all the 8 states. Also verify the correct operation of Reset.

3. Derive the transistor-level implementation of your one-bit modular Up-Down counter cell.

4. Model the transistor-level implementation of your one-bit modular Up-Down counter cell using SPICE and verify its correct functionality.

5. Determine the **worst case propagation delay** across your modular cell assuming that all nMOS transistors with a (W/L) ratio of 2, and all pMOS transistors with a (W/L) ratio of 4. For the register, determine the **setup** and **hold** time and the **FF propagation delay** of your design. Determine the maximum frequency across which your design can work. Verify this by spice simulations. Assume a load capacitor of 0.2 pF at the D-input of the FF and a 0.2 pF at the Q output of the D-FF.

6. Build a 3-bit Up-Down counter in Spice using the one-bit modular Up-Down counter cell as a subcircuit. Verify by simulations the correct operation of the counter. Also, verify that the counter will work properly under the maximum frequency you estimated in (5).

7. Draw the stick diagram layout of your one-bit modular Up-Down counter cell.

8. Using MAGIC, draw the layout of your one-bit modular Up-Down counter cell assuming that all nMOS transistors are with a (W/L) ratio of 2, and all pMOS transistors are with a (W/L) ratio of 4. Assume that the minimum feature size is used for all transistors.

9. Extract one-bit modular Up-Down counter cell of your design from your layout, using the command ***extract***, convert it into the simulator format, using ***ext2sim***, and then simulate it using ***irsim*** and verify that it is working properly.

10. Extract the SPICE model of your one-bit modular Up-Down counter cell, using the command ***ext2spice***. Then, using SPICE, determine the worst-case transition and propagation delay times of your output signals. Estimate the worst-case propagation delay for the 3-bit Up-Down Counter Circuit.

11. Implement the 3-bit Up-Down Counter Circuit based on the one-bit modular Up-Down counter cell that you have designed and draw its layout.

12. Extract the 3-bit Up-Down Counter Circuit of your design and verify its correct functionality using irsim.

13. Extract the SPICE model of the 3-bit Up-Down Counter Circuit and determine the maximum propagation delay across it. Determine the maximum frequency under which your design will work properly. Compare this to the estimated worst-case propagation delay obtained in 5&6. Comment on differences.

14. Write a professional report documenting all the design stages of the 3-bit Up-Down Counter Circuit. All layout plots, circuit diagrams, logic simulations, irsim simulations and SPICE simulation results should be submitted with a final report by the end of the project deadline. Organization and completeness of the report is important.

When extracting your design from Magic, extract it without extracting resistance and capacitances. Add a 0.1 pF on the D and Q inputs of the D-FF. You can do this by running the following sequence of commands from inside magic:
:Extract no resistance
:Extract no capacitance
:Extract

For SPICE simulation, Use the AMI 0.5U, 5V technology file given in the web link **http://www.ccse.kfupm.edu.sa/~aimane/032/coe360/AMI0.5Uparam.txt**

This project is to be carried out by a team of two students. Each student is supposed to work on one component of the design i.e. register and counter combinational logic. The distribution of the project marks is as follows:

Task	**Mark**
Logic design	**5%**
Verification of logic design by simulation	**5%**
Transistor-level design of the modular cell	**5%**
Spice Simulation of transistor-level design and worst case delay estimation for the modular cell	**10%**
Stick diagram layout of the modular cell	**10%**

Magic layout of the modular cell	**10%**
Logic verification of extracted modular cell using irsim	**10%**
Spice simulation of extracted cell and timing analysis	**10%**
Layout design of 3-bit up-down counter circuit	**10%**
Logic simulation of 3-bit up-down counter circuit using irsim	**10%**
Spice simulation of 3-bit up-down counter circuit and timing analysis	**10%**
Report	**5%**
Total	**100%**

This project is to be performed in phases and the **deadline** for the various phases is indicated in the table below:

Phase	**Tasks**	**Deadline**
Logic Design & Simulation	1-2	Wednesday, August 3
Transistor-level Design and Spice Analysis	3-6	Wednesday, August 10
One-Bit Layout Design, Irsim Simulation, and Spice Analysis	7-10	Wednesday, August 17
3-Bit Layout Design, Irsim Simulation, and Spice Analysis & Report	11-14	Wednesday, August 24