COE 360 Principles of VLSI Design
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Power Meter Technique

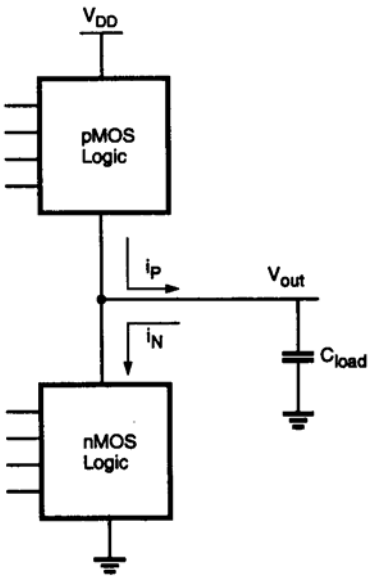


Figure 6.29 Generalized CMOS logic circuit.

predicted by the power-dissipation formula (6.70), since the short-circuit current is not being utilized to charge or discharge the output load capacitor. We must be aware that this additional power-dissipation term can be quite significant under some non-ideal conditions. If the load capacitance is increased, on the other hand, the short-circuit dissipation term usually becomes negligible in comparison to the power dissipation which is due to the charging/discharging of capacitances.

Power Meter Simulation

In the following, we present a simple circuit simulation approach which can be used to estimate the average power dissipation of arbitrary circuits (including the effects of short circuit and leakage currents), under realistic operating conditions. According to (6.66), the average power dissipation of any device or circuit which is driven by a periodic input waveform can be found by integrating the product of its instantaneous terminal voltage and its instantaneous terminal current over one period. If we have to determine the amount of P_{avg} drawn from the power supply over one period, the problem is reduced to finding only the time-average of the power supply current, since the power supply voltage is a constant.

Using a simple simulation model called the *power meter,* we can estimate the average power dissipation of an arbitrary device or circuit driven by a periodic input, with transient circuit simulation. Consider the circuit structure shown in Fig. 6.30, in which a zero-volt independent voltage source is connected in series with the power supply voltage source V_{DD} of the device or circuit in question. Consequently, the

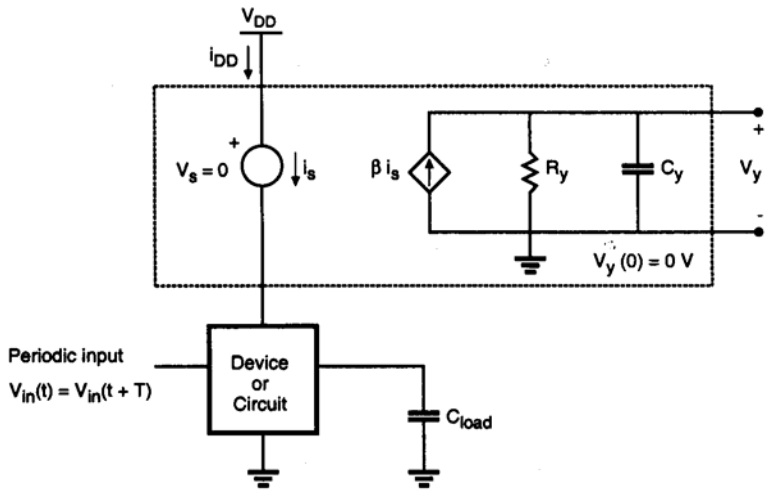


Figure 6.30 The power meter circuit used for the simulation of average dynamic power dissipation of an arbitrary device or circuit.

instantaneous power supply current $i_{DD}(t)$ which is being drawn by the circuit will also pass through the zero-volt voltage source, $i_s(t) = i_{DD}(t)$.

The power meter circuit consists of three elements: a linear current-controlled current source, a capacitor, and a resistor, all connected in parallel. The current equation for the common node of the power meter circuit can be written as follows:

$$C_y \frac{dV_y}{dt} = \beta i_s - \frac{V_y}{R_y} \tag{6.71}$$

The initial condition of the node voltage V_y is set as $V_y(0) = 0\,\text{V}$. Then, the time-domain solution of $V_y(t)$ can be found by integrating (6.71).

$$V_y(t) = \frac{\beta}{C_y} \int_0^t exp\left(-\frac{t-\tau}{R_y C_y}\right) i_{DD}(\tau)\, d\tau \tag{6.72}$$

Assuming $R_y C_y \gg T$, the voltage value $V_y(T)$ at the end of one period can be approximated as follows.

$$V_y(T) \approx \frac{\beta}{C_y} \int_0^T i_{DD}(\tau)\, d\tau \tag{6.73}$$

If the constant coefficient value of the current-controlled current source is set to be

$$\beta = V_{DD} \frac{C_y}{T} \tag{6.74}$$

the voltage value $V_y(T)$ at the end of one period will be found by transient simulation as:

$$V_y(T) = V_{DD} \cdot \frac{1}{T} \int_0^T i_{DD}(\tau)\, d\tau \tag{6.75}$$

Note that the right-hand side of (6.75) corresponds to the average power drawn from the power supply source over one period. Thus, the value of the node voltage V_y at $t = T$ gives the average power dissipation.

The power meter circuit shown in Fig. 6.30 can be easily simulated using a conventional circuit simulation program such as SPICE, and it enables us to accurately estimate the average power dissipation of any circuit with arbitrary complexity. Also note that the power meter circuit inherently takes into account the additional power dissipation due to the short-circuit currents, which may arise because of nonideal input conditions. In the following example, we present a sample SPICE simulation of the power meter for estimating the dynamic power dissipation of a CMOS inverter circuit.

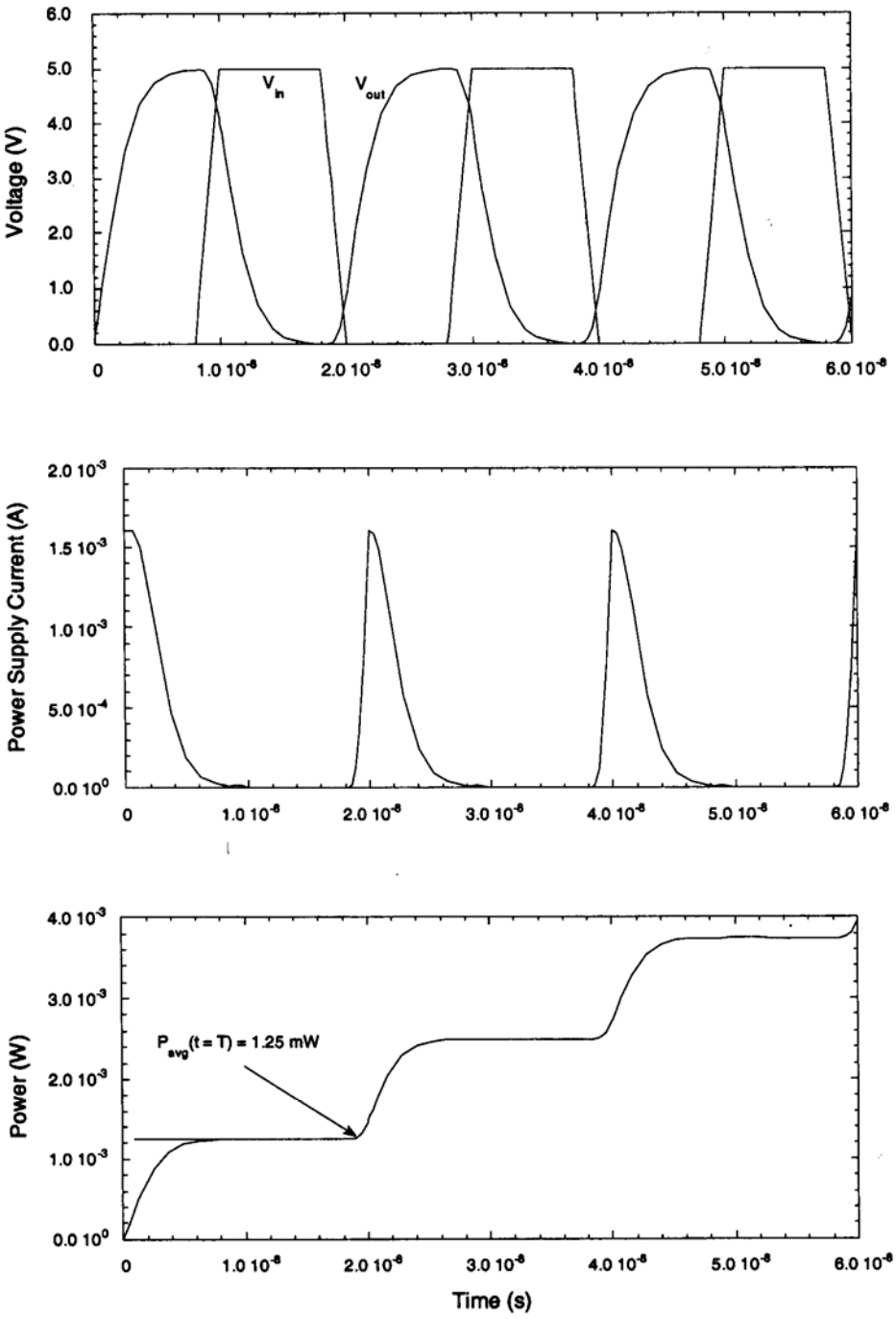
EXAMPLE 6.6

Consider the simple CMOS inverter circuit shown in Fig. 6.27. We will assume that the circuit is being driven by a square-wave input signal with period $T = 20$ ns, and that the total output load capacitance is equal to 1 pF. The power supply voltage is 5 V. Using the average dynamic power-dissipation formula (6.70) derived earlier, we can calculate the expected power dissipation to be $P_{avg} = 1.25$ mW.

Now, the circuit with an attached power meter will be simulated using SPICE. The corresponding circuit input file is listed here for reference. The controlled current source coefficient is calculated as 0.025, according to (6.74). The resistance and capacitance values R_y and C_y are chosen as 100 kΩ and 100 pF to satisfy the condition $R_y C_y \gg T$.

```
Power meter simulation:
mn 3 2 0 0 nmod w=10u l=1u
mp 3 2 4 1 pmod w=20u l=1u
vdd 1 0 5
vtstp 1 4 0
.model nmod nmos(vto=1 kp=20u)
.model pmod pmos(vto=-1 kp=10u)
vin 2 0 pulse(0 5 8n 2n 2n 8n 20n)
cl 3 0 1p
fp 0 9 vtstp 0.025
rp 9 0 100k
cp 9 0 100p
.tran 1n 60n uic
.print tran v(3) v(2)
.print tran i(vtstp)
.print tran v(9)
.end
```

The simulation results are plotted on the following page. It can be seen that here, the significant power supply current is being drawn from the voltage source V_{DD} only during the charge-up phase of the output capacitor. The power meter output voltage by the end of the first period corresponds to exactly 1.25 mW, as expected.


Voltage (V)
6.0
5.0
4.0
3.0
2.0
1.0
0.0
V_{in}
V_{out}
0
1.0 10⁻⁶
2.0 10⁻⁶
3.0 10⁻⁶
4.0 10⁻⁶
5.0 10⁻⁶
6.0 10⁻⁶
Power Supply Current (A)
2.0 10⁻³
1.5 10⁻³
1.0 10⁻³
5.0 10⁻⁴
0.0 10⁰
Power (W)
4.0 10⁻³
3.0 10⁻³
2.0 10⁻³
1.0 10⁻³
0.0 10⁰
$P_{avg}(t = T) = 1.25$ mW
Time (s)