COE 360 Principles of VLSI Design
Dr. Aiman El-Maleh

Lecture#7

Threshold Voltage & Current Equations

1. Threshold voltage
2. MOS current equations
3. V-I characteristics of MOS transistors

Threshold Voltage :

The threshold voltage, V_t, for an MOS transistor can be defined as the voltage applied between the gate and the source of an MOS device below which the drain-to-source current is nearly zero.

- $V_t = V_{t\text{-}MOS} + V_{fb}$

$V_{t\text{-}MOS}$ is the ideal threshlod voltage of a MOS capacitor where there is no work function difference between the gate and substrate materials.

$$V_{t\text{-}MOS} = 2\phi_b + \frac{Q_b}{C_{ox}}$$

where $\phi_b = \frac{KT}{q} \ln\left(\frac{N_A}{N_i}\right)$ is the bulk potential, a term that accounts for the doping of the substrate.

N_A : density of carriers in the doped substrate
N_i : density of carriers in intrinsic silicon

$Q_b = \sqrt{2 \varepsilon_{si} q N_A 2 \phi_b}$ is the bulk charge

ε_{si} is the permitivity of silicon = 1.06×10^{-12} Farads/cm.

$\frac{KT}{q}$ = 0.02586 volts at 300°K.

- C_{ox} is the oxide capacitance

  $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, where ε_{ox} is the permitivity of oxide, and t_{ox} is the gate-oxide thickness

- The flat band voltage $\boxed{V_{fb} = Q_{ms} - \frac{Q_{fc}}{C_{ox}}}$

* Q_{ms} is the work function difference between the gate material and the silicon substrate ($\Phi_{gate} - \Phi_{si}$).

* Q_{fc} represents the surface state charge due to imperfections in the silicon oxide interface and doping.

- For n-transistor : $Q_{ms} = -\left(\frac{E_g}{2} + \Phi_b\right) \simeq -0.9\,V$
- For p-transistor : $Q_{ms} = -\left(\frac{E_g}{2} - \Phi_b\right) \simeq -0.2\,V$

(assuming $N_A = 1 \times 10^{16}\ cm^{-3}$)

E_g is the band gap energy of silicon which decreases with temperature.

* Thus the threshold voltage can be varied by changing:
  - the doping concentration of the substrate (N_A)
  - the oxide capacitance, C_{ox}
  - the surface state charge (Q_{fc})

- Two common techniques used for the adjustment of the threshold voltage:
  (1) By varying the doping at the silicon insulator interface through ion implantation (i.e. affecting Q_{fc})
  (2) Using different insulating material for the gate (i.e. affecting C_{ox}).

MOS Device Design Equations:

MOS transistors have three regions of operation:

- Cutoff or subthreshold region
- Nonsaturation or linear region
- Saturation region

The ideal first order equations describing the behavior of an nMOS device in the three regions are:

(1) The cutoff region:

$$I_{ds} = 0 \qquad V_{gs} \leq V_t$$

(2) The nonsaturation, linear, or triode region:

$$I_{ds} = \beta \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$0 < V_{ds} < V_{gs} - V_t$$

(3) The saturation region:

$$I_{ds} = \beta \frac{(V_{gs} - V_t)^2}{2} \qquad 0 < V_{gs} - V_t \leq V_{ds}$$

I_{ds} : drain-to-source current

V_{gs} : gate-to-source voltage

V_t : threshold voltage

β : mos transistor gain factor

* $\beta = \frac{\mu \varepsilon}{t_{ox}} \left(\frac{W}{L} \right)$ i.e. the gain factor is dependent on the process parameters and the device geometry.

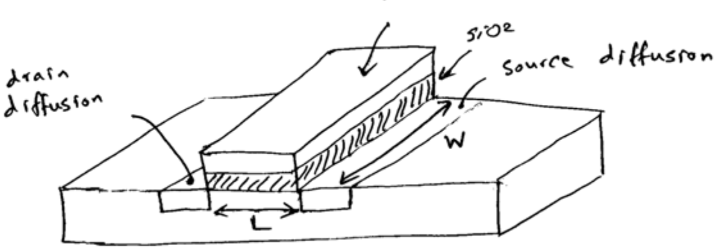
μ : effective surface mobility of the carriers in the channel

ε : permitivity of the gate insulator

t_{ox} : thickness of the gate insulator

W : width of the channel

L : length of the channel



- VI characteristics of MOS transistors: