COE 360 Principles of VLSI Design
Dr. Aiman El-Maleh

Lecture#6

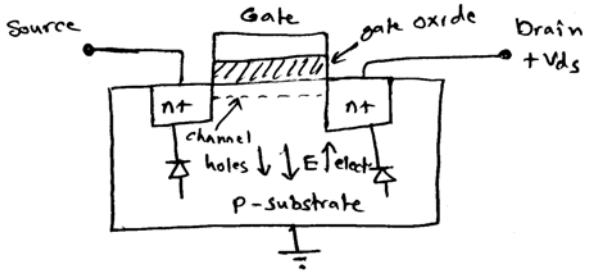
MOS Transistor Theory

1. Accumulation mode
2. Depletion mode
3. Inversion mode
4. Transistor operation regions: Linear and saturated modes

COE 360: Lec # 6 Dr. Aiman EL-Maleh

- Mos transistor theory:

* Structure of n-mos type enhancement transistor

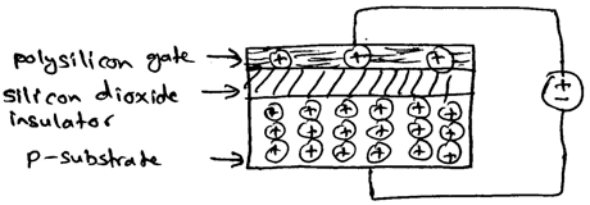


- With zero gate bias ($V_{gs}=0$), no current flows from drain to source because they are effectively insulated from each other by the two reverse biased pn junctions.

- However, when $V_{gs}>0$, this produces an electric field E across the substrate, which attracts electrons toward the gate and repels holes.

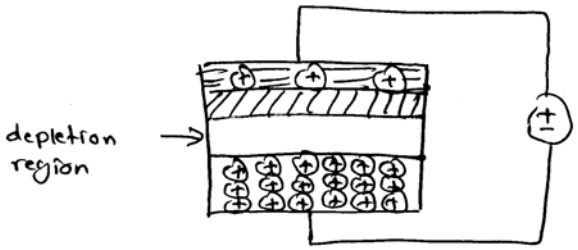
- If V_{gs} is sufficiently large, the region under the gate changes from p-type to n-type (due to accumulation of attracted electrons) and provides a conduction path between the source and the drain.
Under such a condition, the surface of the underlying p-type silicon is said to be inverted and the channel formed is called n-channel.

- Accumulation mode : $V_{gs} \ll V_T$



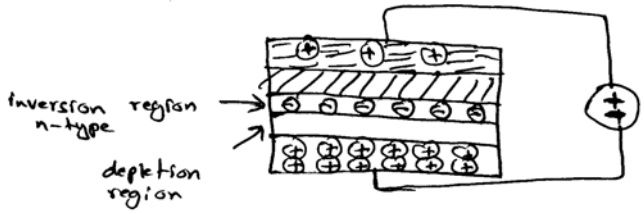
initially, the p-substrate has holes, and when $V_{gs} \ll V_T$ nothing happens.

- Depletion mode : $V_{gs} \simeq V_T$



When V_{gs} is raised above V_T in potential, the holes are repelled causing a depletion region under the gate.

- Inversion mode : $V_{gs} > V_T$

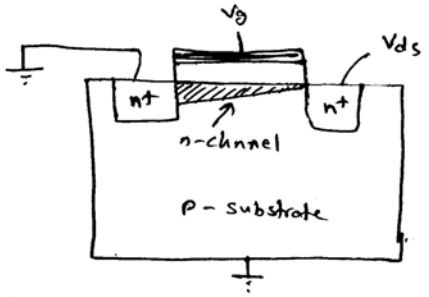


When V_{gs} is raised further above V_T, electrons are attracted under the gate. This forms a conductive layer of electrons in the p-substrate.

- Initially, when $V_{gs} > V_T$ and $V_{DS} > 0$, the channel will be established and the drain-to-source voltage is responsible for sweeping the electrons from the source toward the drain.

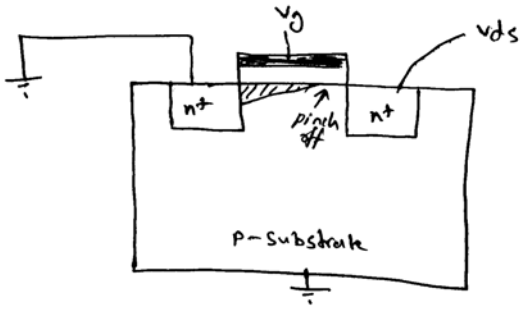
- At the source end of the channel, the full gate voltage is effective in inverting the channel. However, at the drain end of the channel, only the difference between the gate and drain voltages is effective.

- When $V_{gs} - V_T > V_{DS}$ i.e., $V_{gD} > V_T$, the channel is in the linear or nonsaturated region where the channel current I_{DS} is a function of both gate and drain voltages.



- When $V_{gs} - V_T < V_{DS}$ i.e., $V_{gD} < V_T$, the channel becomes pinched off — the channel no longer reaches the drain. However, in this case, conduction is brought about by a drift mechanism of electrons under the influence of positive drain voltage.

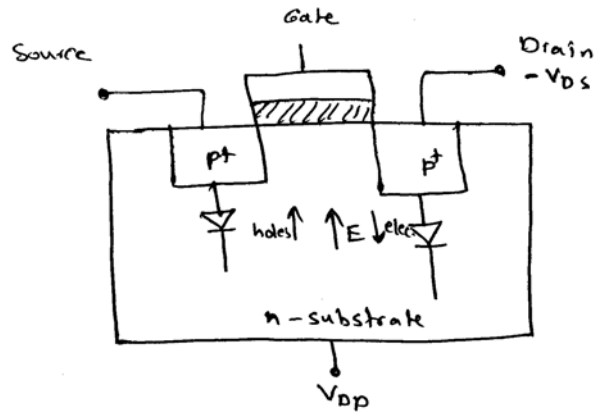
As the electrons leave the channel, they are injected into the drain depletion region and are subsequently accelerated toward the drain. The voltage across the pinched-off channel tends to remain fixed at $(V_{gs} - V_T)$. This condition is the saturated state in which the channel current is controlled by the gate voltage and is almost independent of the drain voltage.



$V_{gD} < V_T$

- Cutoff region: channel flow is essentially zero (accumulation region)
- Nonsaturated region: $V_{gd} \geq V_T$, the drain current is dependent on the gate and drain voltages.
- Saturated region: $V_{gd} \leq V_T$, the drain current is independent of the drain voltage.

- pmos Enhancement transistor:



Application of a negative gate voltage (with respect to source) draws holes into the region below the gate resulting in the channel changing from the n-type to the p-type. Thus, a conduction path is created between the source and the drain. Conduction results from the movement of holes in the channel. A negative drain voltage sweeps holes from the source through the channel to the drain.