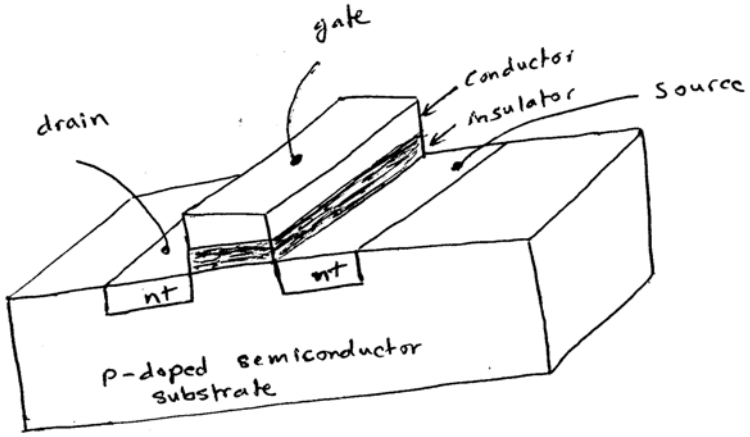
COE 360 Principles of VLSI Design
Dr. Aiman El-Maleh

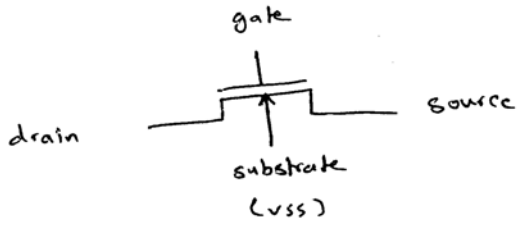
Lecture#4

Logic Design using CMOS

1. NMOS transistor basic structure
2. PMOS transistor basic structure
3. Transmission gate
4. Nand gate
5. Nor gate
6. CMOS gates

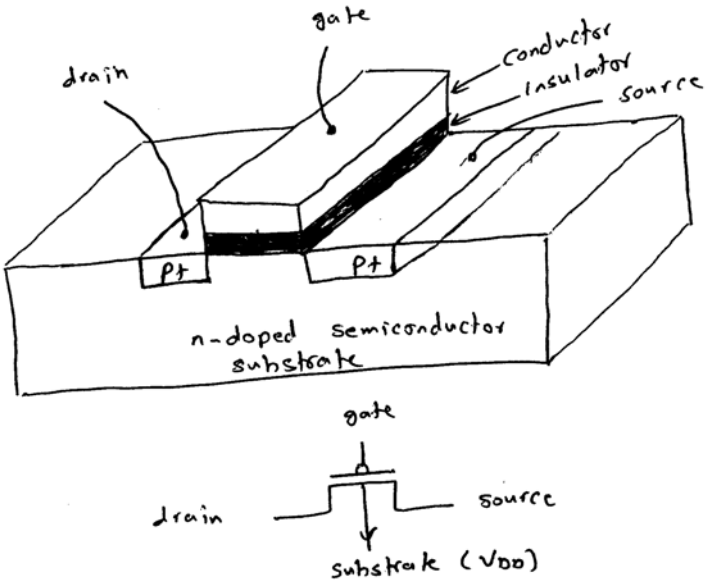
- n-transistor (nMos):





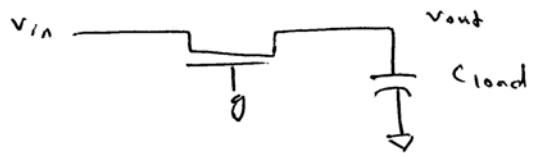
- An MOS (metal-oxide-silicon) structure is created by superimposing several layers of conducting, insulating, and transistor forming materials.
- CMOS technology provides two types of transistors, an n-type transistor (nMOS) and a p-tye transistor (pMOS).

- p-transistor (pMOS)



- gate is a control input - it affects the flow of current between the source and drain.
- In an nmos transistor, the source is the one with lower voltage (source of negative charges.
- In a pmos transistor, the source is the one with higher voltage (source of positive charges).

- An nmos transistor produces a good 0 but a poor 1

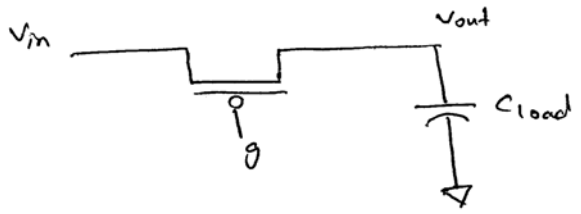


* An nmos transistor conducts if the potential difference between the gate and the source $V_{gs} > V_T$ (threshold voltage) ($V_T > 0$)
* Source is like the substrate i.e. the node with potential Vss.
* If $V_g = V_{ss}$ (low), then regardless of the values on Vin & Vout, the transistor will be off since $V_{gs} < V_T$. Thus, Vout will be floating and has a high impedance value Z.
* If $V_g = V_{DD}$, $V_{in} = V_{ss}$, and $V_{out} = V_{DD}$, the transistor will be on since $V_{gs} = V_{DD} > V_T$ until all the charge on Vout is eliminated and $V_{out} = V_{ss}$. Thus, we get a good 0.
* If $V_g = V_{DD}$, $V_{in} = V_{DD}$, and $V_{out} = V_{ss}$, then Vout will be the source and Vin the drain, and current will flow from Vin to Vout and the capacitance will start charging.

The transistor will continue conducting as long as V_{gs}, the potential difference between the gate and $V_{out} > V_T$. At the point wher $V_{out} = V_{DD} - V_T$, V_{gs} becomes equal to V_T and the transistor ceases conduction.

Thus, the maximum value that V_{out} can get is $V_{DD} - V_T$, which is a poor 1.

- A pmos transistor produces a good 1 but a poor 0.

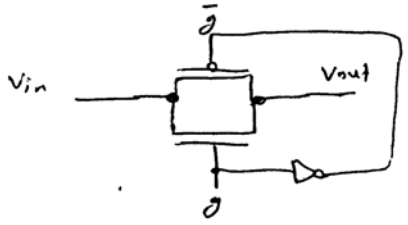


* A pmos transistor conducts if the potential difference between the gate and the source $V_{gs} < +V_T$. ($V_T < 0$)
* Source is the terminal connected to V_{DD}
* If $V_g = V_{DD}$ (high), then regardless of the values on Vin & Vout, the transistor will be off since $V_{gs} > +V_T$. Thus, Vout will be floating and has a high impedance value Z.

* If $V_g = V_{SS}$ (low), and $V_{in} = V_{DD}$, the transistor will be on since the potential difference between the gate and V_{in} (source) $= -V_{DD} < +V_T$. Thus, current flows and charges the capacitor towards V_{DD}, and we get a good 1.

* If $V_g = V_{SS}$, and $V_{in} = V_{SS}$, and $V_{out} = V_{DD}$, V_{out} in this case will be the source and V_{in} the drain. Since $V_{gs} = -V_{DD} < +V_T$ the transistor will be on and the load capacitor discharges until $V_{out} = V_T$, at which point the transistor ceases conducting since $V_{gs} = +V_T$. Thus, the p-transistor produces a poor 0 equal to V_T.

- To obtain both a good 0 and a good 1, we combine an n-transistor and a p-transistor in parallel as shown below:



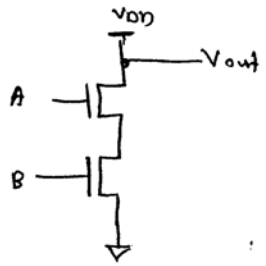
This switch is called a complementary switch or C-switch, transmission gate or pass gate.

* If $V_g = V_{ss}$, both the n and p transistors will be off.

* If $V_g = V_{DD}$, $V_{in} = V_{ss}$, and $V_{out} = V_{DD}$ both transistors will be on, and the load capacitance on Vout will discharge. However, when $V_{out} = V_T$, the p-transistor stops conducting while the n-mos transistor continues conducting until $V_{out} = V_{ss}$. So, we get a good 0.

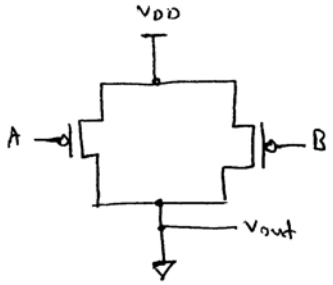
* If $V_g = V_{DD}$, $V_{in} = V_{DD}$, and $V_{out} = V_{ss}$ both transistors will be on, and the load capacitance on Vout will charge. However, when $V_{out} = V_{DD} - V_T$, the n-trans. stops conducting while the p-transistor continues conduction and we get $V_{out} = V_{DD}$. So, we get a good 1.

- NAND gate:



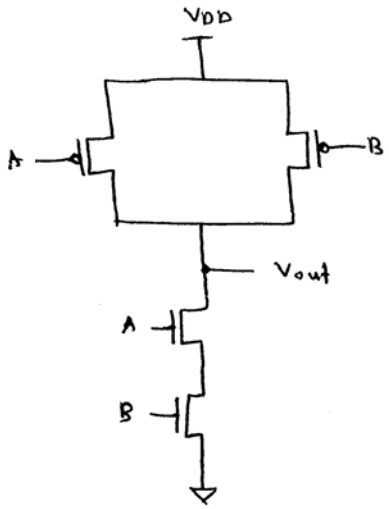
$V_{out} = (A \cdot B)'$

nmos



$V_{out} = \bar{A} + \bar{B} = (A \cdot B)'$

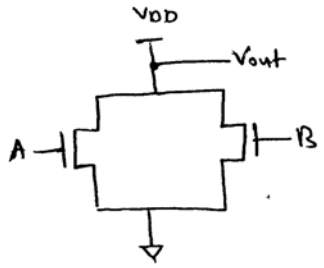
pmos



$V_{out} = (A \cdot B)'$

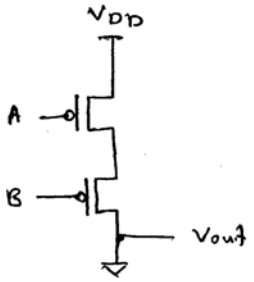
cmos

- NOR gate:



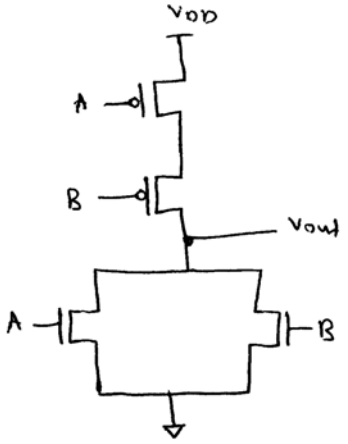
$V_{out} = (A + B)'$

nmos



$V_{out} = \overline{A} \cdot \overline{B} = (A + B)'$

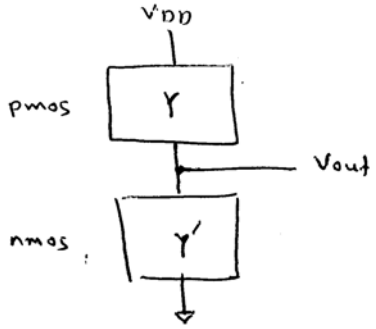
pmos



$V_{out} = (A + B)'$

CMOS

- CMOS gates:



To implement a function Y in cmos, implement in the lower part $\overline{Y}$ using nmos and in the upper part Y using pmos.

Example: Implement $Y = (A \cdot B + C \cdot D)'$

$\overline{Y} = AB + CD$, $Y = (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$