COE 360 Principles of VLSI Design
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Lecture#3

Basic Specifications of Digital Circuits

1. Voltage Transfer Characteristic of NMOS Inverter
2. VOH, VOL, VIH, VIL
3. Noise Margin
4. Static Power Dissipation
5. Fanout, Fanin

COE 360 : Lec#3

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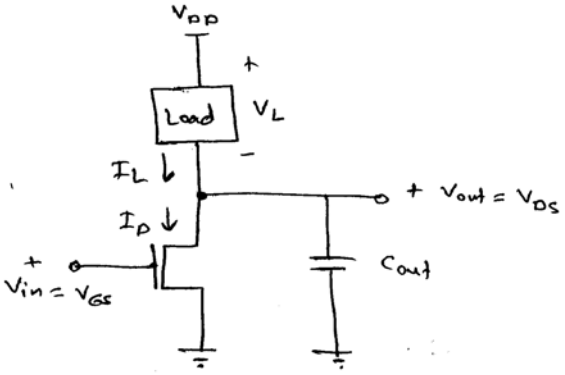
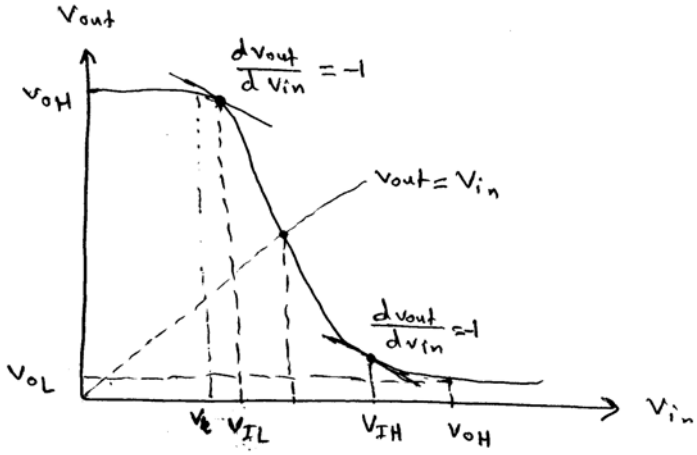
- Basic specifications of Digital Circuits:



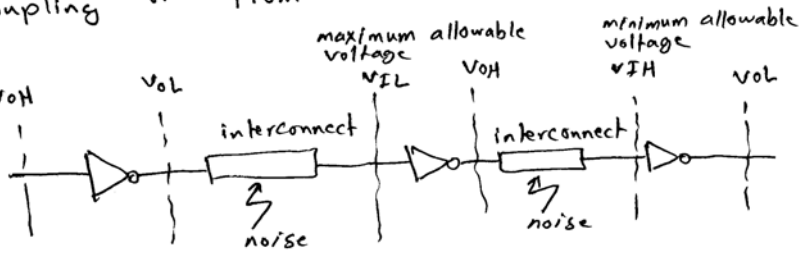
nmos inverter

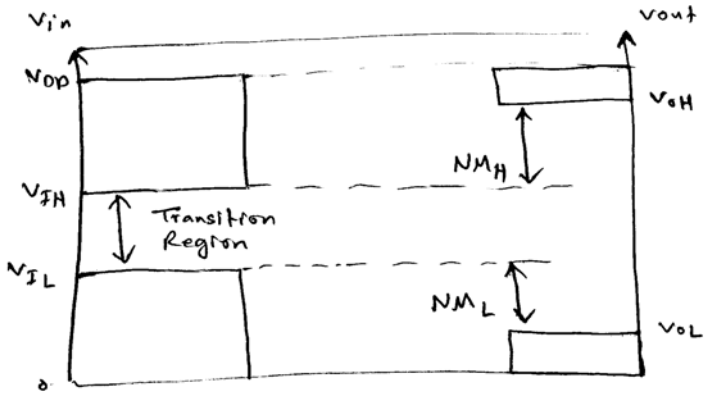


Voltage transfer characteristic of nmos inverter

- V_{OH} : maximum output voltage when the output level is logic "1".
- V_{OL} : minimum output voltage when the output level is logic "0".
- V_{IL} : maximum input voltage which can be interpreted as logic "0".
- V_{IH} : minimum input voltage which can be interpreted as logic "1".

- Circuit noise : corresponds to unwanted signals that are coupled to some part of the circuit from neighboring lines by capacitive or inductive coupling or from outside of the system.





- $NM_L = V_{IL} - V_{OL}$
- $NM_H = V_{OH} - V_{IH}$

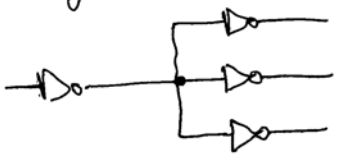
* Power Dissipation

$$P_{DC} = V_{DD} \cdot I_{DC}$$

Assuming that the input voltage level corresponds to "0" during 50% of the operation time and to logic "1" during the other 50%, the overall power consumption

$$P_{DS} = \frac{V_{DD}}{2} \left[I_{DC}(V_{in} = low) + I_{DC}(V_{in} = High) \right]$$

* Fan-out : describes the number of load gates, of similar design connected to the output of a driver gate.



fanout = 3

* Fan-in : describes the number of gates connected to the inputs of a gate.

Inputs		Output
x	y	z
L	L	H
L	H	L
H	L	L
H	H	L

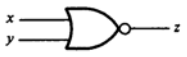


FIGURE 10-2
Positive logic NOR gate

CMOS, employ a type of unipolar transistor called a metal-oxide-semiconductor field-effect transistor, abbreviated MOSFET or MOS for short.

In this chapter, we first introduce the most common characteristics by which the digital logic families are compared. We then describe the properties of the bipolar transistor and analyze the basic gates in the bipolar logic families. We then explain the operation of the MOS transistor and introduce the basic gates of its two logic families.

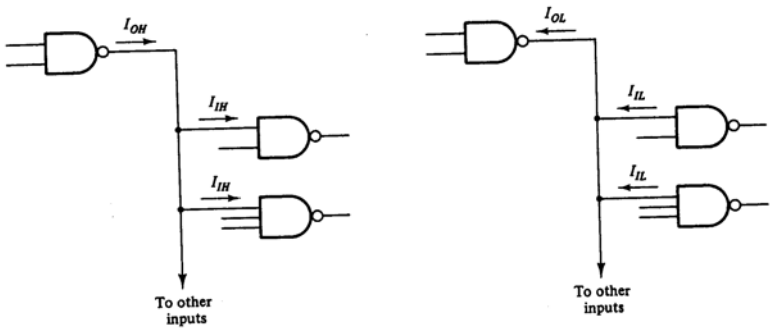
10-2 SPECIAL CHARACTERISTICS

The characteristics of IC digital logic families are usually compared by analyzing the circuit of the basic gate in each family. The most important parameters that are evaluated and compared are fan-out, power dissipation, propagation delay, and noise margin. We first explain the properties of these parameters and then use them to compare the IC logic families.

Fan-Out

The fan-out of a gate specifies the number of standard loads that can be connected to the output of the gate without degrading its normal operation. A standard load is usually defined as the amount of current needed by an input of another gate in the same logic family. Sometimes the term *loading* is used instead of fan-out. This term is derived because the output of a gate can supply a limited amount of current, above which it ceases to operate properly and is said to be overloaded. The output of a gate is usually connected to the inputs of other gates. Each input consumes a certain amount of current from the gate output, so that each additional connection adds to the load of the gate. Loading rules are sometimes specified for a family of digital circuits. These rules give the maximum amount of loading allowed for each output of each circuit in the family. Exceeding the specified maximum load may cause a malfunction because the circuit cannot supply the power demanded from it. The fan-out is the maximum number of inputs that can be connected to the output of a gate, and is expressed by a number.

The fan-out is calculated from the amount of current available in the output of a gate and the amount of current needed in each input of a gate. Consider the connections shown in Fig. 10-3. The output of one gate is connected to one or more inputs of other gates. The output of the gate is in the high voltage level in Fig. 10-3(a). It provides a



(a) High-level output

(b) Low-level output

FIGURE 10-3
Fan-out computation

current source I_{OH} to all the gate inputs connected to it. Each gate input requires a current I_{IH} for proper operation. Similarly, the output of the gate is in the low voltage level in Fig. 10-3(b). It provides a current sink I_{OL} for all the gate inputs connected to it. Each gate input supplies a current I_{IL}. The fan-out of the gate is calculated from the ratio I_{OH}/I_{IH} or I_{OL}/I_{IL}, whichever is smaller. For example, the standard TTL gates have the following values for the currents:

$$I_{OH} = 400\ \mu A$$
$$I_{IH} = 40\ \mu A$$
$$I_{OL} = 16\ mA$$
$$I_{IL} = 1.6\ mA$$

The two ratios give the same number in this case:

$$\frac{400\ \mu A}{40\ \mu A} = \frac{16\ mA}{1.6\ mA} = 10$$

Therefore, the fan-out of standard TTL is 10. This means that the output of a TTL gate can be connected to no more than ten inputs of other gates in the same logic family. Otherwise, the gate may not be able to drive or sink the amount of current needed from the inputs that are connected to it.

Power Dissipation

Every electronic circuit requires a certain amount of power to operate. The power dissipation is a parameter expressed in milliwatts (mW) and represents the amount of power needed by the gate. The number that represents this parameter does not include the

power delivered from another gate; rather, it represents the power delivered to the gate from the power supply. An IC with four gates will require, from its power supply, four times the power dissipated in each gate.

The amount of power that is dissipated in a gate is calculated from the supply voltage V_{CC} and the current I_{CC} that is drawn by the circuit. The power is the product $V_{CC} \times I_{CC}$. The current drain from the power supply depends on the logic state of the gate. The current drawn from the power supply when the output of the gate is in the high-voltage level is termed I_{CCH}. When the output is in the low-voltage level, the current is I_{CCL}. The average current is

$$I_{CC}(\text{avg}) = \frac{I_{CCH} + I_{CCL}}{2}$$

and is used to calculate the average power dissipation:

$$P_D(\text{avg}) = I_{CC}(\text{avg}) \times V_{CC}$$

For example, a standard TTL NAND gate uses a supply voltage V_{CC} of 5 V and has current drains $I_{CCH} = 1$ mA and $I_{CCL} = 3$ mA. The average current is $(3 + 1)/2 = 2$ mA. The average power dissipation is $5 \times 2 = 10$ mW. An IC that has four NAND gates dissipates a total of $10 \times 4 = 40$ mW. In a typical digital system there will be many ICs, and the power required by each IC must be considered. The total power dissipation in the system is the sum total of the power dissipated in all ICs.

Propagation Delay

The propagation delay of a gate is the average transition-delay time for the signal to propagate from input to output when the binary signal changes in value. The signals through a gate take a certain amount of time to propagate from the inputs to the output. This interval of time is defined as the propagation delay of the gate. Propagation delay is measured in nanoseconds (ns). 1 ns is equal to 10^{-9} of a second.

The signals that travel from the inputs of a digital circuit to its outputs pass through a series of gates. The sum of the propagation delays through the gates is the total delay of the circuit. When speed of operation is important, each gate must have a short propagation delay and the digital circuit must have a minimum number of gates between inputs and outputs.

The average propagation delay time of a gate is calculated from the input and output waveforms, as shown in Fig. 10-4. The signal-delay time between the input and output when the output changes from the high to the low level is referred to as t_{PHL}. Similarly, when the output goes from the low to the high level, the delay is t_{PLH}. It is customary to measure the time between the 50 percent point on the input and output transitions. In general, the two delays are not the same, and both will vary with loading conditions. The average propagation-delay time is calculated as the average of the two delays.

As an example, the delays for a standard TTL gate are $t_{PHL} = 7$ ns and $t_{PLH} = 11$ ns. These quantities are given in the TTL data book and are measured with a load resistance of 400 ohms and a load capacitance of 15 pF. The average propagation delay of the TTL gate is $(11 + 7)/2 = 9$ ns.

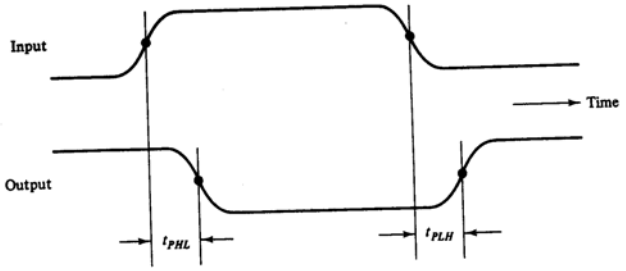


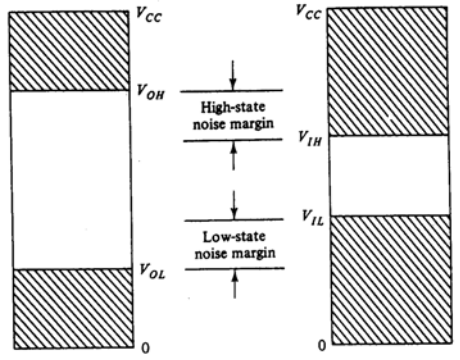
FIGURE 10-4
Measurement of propagation delay

Under certain conditions, it is more important to know the maximum delay time of a gate rather than the average value. The TTL data book lists the following maximum propagation delays for a standard NAND gate: t_{PHL} = 15 ns and t_{PLH} = 22 ns. When speed of operation is critical, it is necessary to take into account the maximum delay to ensure proper operation.

The input signals in most digital circuits are applied simultaneously to more than one gate. All the gates that are connected to external inputs constitute the first logic level of the circuit. Gates that receive at least one input from an output of a first-level gate are considered to be in the second logic level, and similarly for the third and higher logic levels. The total propagation delay of the circuit is equal to the propagation delay of a gate times the number of logic levels in the circuit. Thus, a reduction in the number of logic levels results in a reduction of signal delay and faster circuits. The reduction of the propagation delay in circuits may be more important than the reduction of the total number of gates if speed of operation is a major factor.

Noise Margin

Spurious electrical signals from industrial and other similar sources can induce undesirable voltages on the connecting wires between logic circuits. These unwanted signals are referred to as *noise*. There are two types of noise to be considered. DC noise is caused by a drift in the voltage levels of a signal. AC noise is a random pulse that may be created by other switching signals. Thus, noise is a term used to denote an undesirable signal that is superimposed upon the normal operating signal. *Noise margin* is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. The ability of circuits to operate reliably in a noise environment is important in many applications. Noise margin is expressed in volts and represents the maximum noise signal that can be tolerated by the gate.



(a) Output voltage range (b) Input voltage range

FIGURE 10-5
Signals for evaluating noise margin

The noise margin is calculated from knowledge of the voltage signal available in the output of the gate and the voltage signal required in the input of the gate. Figure 10-5 illustrates the signals for computing noise margin. Part (a) shows the range of output voltages that can occur in a typical gate. Any voltage in the gate output between V_{CC} and V_{OH} is considered as the high-level state and any voltage between 0 and V_{OL} in the gate output is considered as the low-level state. Voltages between V_{OL} and V_{OH} are indeterminate and do not appear under normal operating conditions except during transition between the two levels. The corresponding two voltage ranges that are recognized by the input of the gate are indicated in Fig. 10-5(b). In order to compensate for any noise signal, the circuit must be designed so that V_{IL} is greater than V_{OL} and V_{IH} is less than V_{OH}. The noise margin is the difference $V_{OH} - V_{IH}$ or $V_{IL} - V_{OL}$, whichever is smaller.

As illustrated in Fig. 10-5, V_{OL} is the maximum voltage that the output can be when in the low-level state. The circuit can tolerate any noise signal that is less than the noise margin ($V_{IL} - V_{OL}$) because the input will recognize the signal as being in the low-level state. Any signal greater than V_{OL} plus the noise-margin figure will send the input voltage into the indeterminate range, which may cause an error in the output of the gate. In a similar fashion, a negative-voltage noise greater than $V_{OH} - V_{IH}$ will send the input voltage into the indeterminate range.

The parameters for the noise margin in a standard TTL NAND gate are V_{OH} = 2.4 V, V_{OL} = 0.4 V, V_{IH} = 2 V, and V_{IL} = 0.8 V. The high-state noise margin is 2.4 − 2 = 0.4 V, and the low-state noise margin is 0.8 − 0.4 = 0.4 V. In this case, both values are the same.