COE 360 Principles of VLSI Design
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Lecture#16

Inverter-Equivalent Circuits

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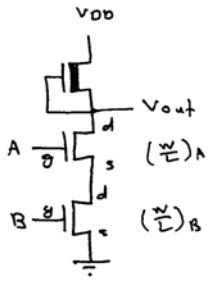
Inverter – Equivalent Circuits

Let us first consider the depletion-load NAND gate shown below.



$$I_{D,A} = \frac{1}{2}\left(\frac{W}{L}\right)_A \mu_n C_{ox}\left[2(V_{GS,A}-V_T)V_{DS,A} - V_{DS,A}^2\right]$$

$$I_{D,B} = \frac{1}{2}\left(\frac{W}{L}\right)_B \mu_n C_{ox}\left[2(V_{GS,B}-V_T)V_{DS,B} - V_{DS,B}^2\right]$$

It is assumed here that $V_{T,A} = V_{T,B} = V_T$, and that $(\mu_n C_{ox})_A = (\mu_n C_{ox})_B$.

Note that $V_{GS,A} = V_{GS,B} - V_{DS,B}$, and that $V_{DS,A} = V_{out} - V_{DS,B}$

$$I_{D,A} = \frac{1}{2}\left(\frac{W}{L}\right)_A \mu_n C_{ox}\left[2(V_{GS,B} - V_{DS,B} - V_T)(V_{out} - V_{DS,B}) - (V_{out} - V_{DS,B})^2\right]$$

$$\Rightarrow I_{D,A} = \frac{1}{2}\left(\frac{W}{L}\right)_A \mu_n C_{ox} \left[2(V_{GS,B} - V_T)(V_{out} - V_{DS,B}) - 2(V_{DS,B})(V_{out} - V_{DS,B}) - (V_{out} - V_{DS,B})^2 \right]$$

$$\Rightarrow I_{D,A} = \frac{1}{2}\left(\frac{W}{L}\right)_A \mu_n C_{ox} \left[2(V_{GS,B} - V_T) V_{out} - 2(V_{GS,B} - V_T) V_{DS,B} - 2 V_{DS,B} V_{out} + 2 V_{DS,B}^2 - V_{out}^2 + 2 V_{out} V_{DS,B} - V_{DS,B}^2 \right]$$

$$\Rightarrow I_{D,A} = \frac{1}{2}\left(\frac{W}{L}\right)_A \mu_n C_{ox} \left[2(V_{GS,B} - V_T) V_{out} - V_{out}^2 - \left[2(V_{GS,B} - V_T) V_{ds,B} - V_{DS,B}^2 \right] \right]$$

$$\Rightarrow I_{D,A} = \frac{1}{2}\left(\frac{W}{L}\right)_A \mu_n C_{ox} \left[\frac{I_{D,eq}}{\frac{1}{2}\left(\frac{W}{L}\right)_{eq} \mu_n C_{ox}} - \frac{I_{D,B}}{\frac{1}{2}\left(\frac{W}{L}\right)_B \mu_n C_{ox}} \right]$$

$$\Rightarrow \frac{I_{D,A}}{\frac{1}{2}\left(\frac{W}{L}\right)_A \mu_n C_{ox}} = \frac{I_{D,eq}}{\frac{1}{2}\left(\frac{W}{L}\right)_{eq} \mu_n C_{ox}} - \frac{I_{D,B}}{\frac{1}{2}\left(\frac{W}{L}\right)_B \mu_n C_{ox}}$$

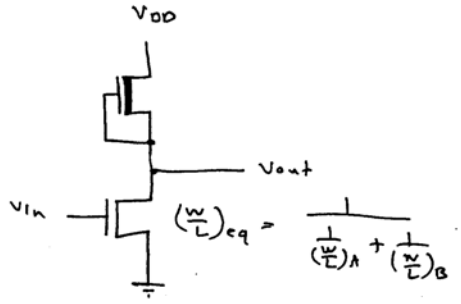
$$\Rightarrow \frac{I_{D,eq}}{\frac{1}{2}\left(\frac{W}{L}\right)_{eq}\mu_n C_{ox}} = \frac{I_{D,A}}{\frac{1}{2}\left(\frac{W}{L}\right)_A \mu_n C_{ox}} + \frac{I_{D,B}}{\frac{1}{2}\left(\frac{W}{L}\right)_B \mu_n C_{ox}}$$

Note that $I_{D,A} = I_{D,B} = I_{D,eq}$

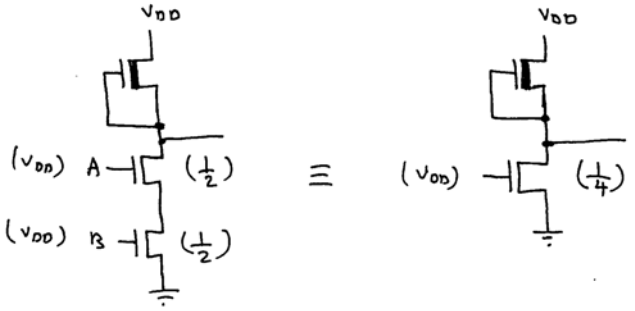
$$\Rightarrow \frac{1}{\left(\frac{W}{L}\right)_{eq}} = \frac{1}{\left(\frac{W}{L}\right)_A} + \frac{1}{\left(\frac{W}{L}\right)_B}$$

$$\Rightarrow \left(\frac{W}{L}\right)_{eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_A} + \frac{1}{\left(\frac{W}{L}\right)_B}}$$

Thus, the inverter equivalent to the 2-input NAND gate assuming both inputs have the same value is shown below

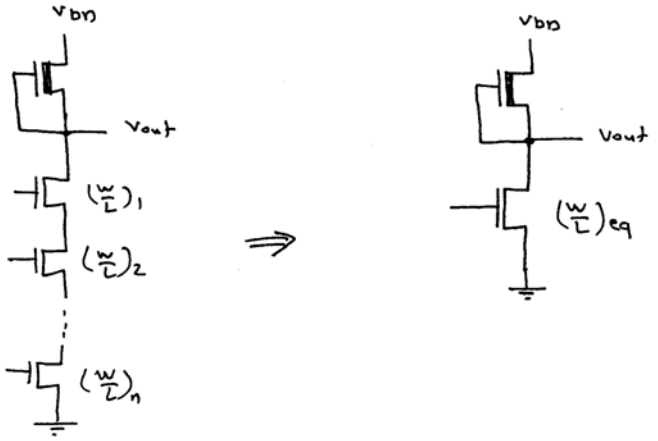


For example,



For a gereralized n-input NAND gates, which consists of n serres connected driver transistors, the $(\frac{W}{L})$ ratro of the equivalent driver transistor is

$$\left(\frac{W}{L}\right)_{equivalent} = \frac{1}{\sum_{K(on)} \frac{1}{\left(\frac{W}{L}\right)_K}}$$



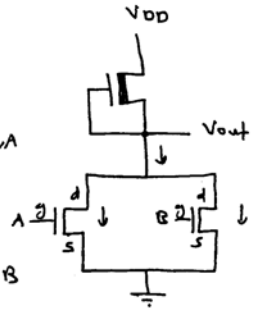
Note that we have neglected the substrate-bias effect, and assumed that the threshold voltages of all transistors equals to V_T.

If the series-connected transistors are identical i.e., $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \cdots = \left(\frac{W}{L}\right)_n$, the width-to-length ratio of the equivalent transistor becomes

$$\left(\frac{W}{L}\right)_{equivalent} = \frac{1}{n}\left(\frac{W}{L}\right)$$

- NOR gates

Let us consider the 2-input NOR gate shown below.



Note that $I_D = I_{D,A} + I_{D,B}$

$$I_{D,A} = \frac{1}{2}\left(\frac{W}{L}\right)_A \mu_n C_{ox}\left[2(V_{GS,A} - V_t)V_{DS,A} - V_{DS,A}^2\right]$$

$$I_{D,B} = \frac{1}{2}\left(\frac{W}{L}\right)_B \mu_n C_{ox}\left[2(V_{GS,B} - V_t)V_{DS,B} - V_{DS,B}^2\right]$$

Note that $V_{gs,A} = V_{gs,B} = V_{GS}$ and that

$V_{DS,A} = V_{DS,B} = V_{out}$

$$\Rightarrow \frac{1}{2}\left(\frac{W}{L}\right)_{eq} \mu_n C_{ox}\left[2(V_{GS}-V_t)V_{out} - V_{out}^2\right]$$

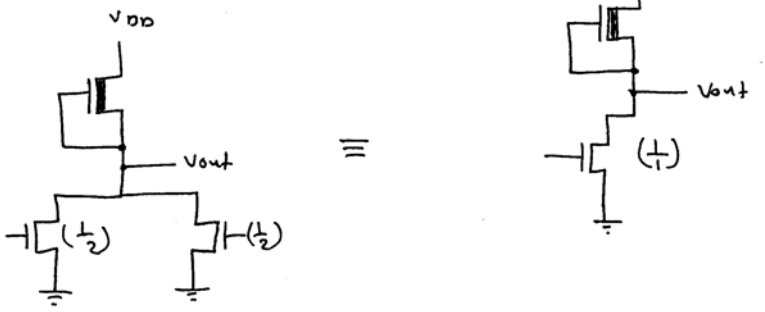
$$= \frac{1}{2}\left(\frac{W}{L}\right)_A \mu_n C_{ox}\left[2(V_{GS}-V_t)V_{out} - V_{out}^2\right]$$

$$+ \frac{1}{2}\left(\frac{W}{L}\right)_B \mu_n C_{ox}\left[2(V_{GS}-V_t)V_{out} - V_{out}^2\right]$$

$$= \frac{1}{2}\left[\left(\frac{W}{L}\right)_A + \left(\frac{W}{L}\right)_B\right]\mu_n C_{ox}\left[2(V_{GS}-V_t)V_{out} - V_{out}^2\right]$$

$$\Rightarrow \left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L}\right)_A + \left(\frac{W}{L}\right)_B$$

For example,

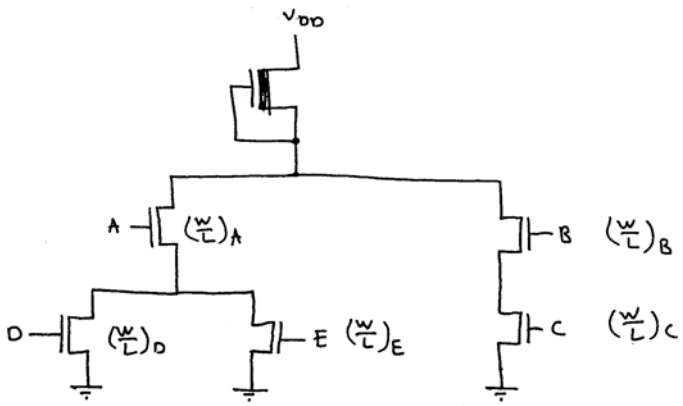


Thus, an n-input NOR gate can be reduced to an equivalent inverter with the following $\left(\frac{W}{L}\right)$ ratio:

$$\left(\frac{W}{L}\right)_{equivalent} = \sum_{K(on)} \left(\frac{W}{L}\right)_K$$

Example

Find the inverter-equivalent of the following circuit assuming all inputs are logic-high.

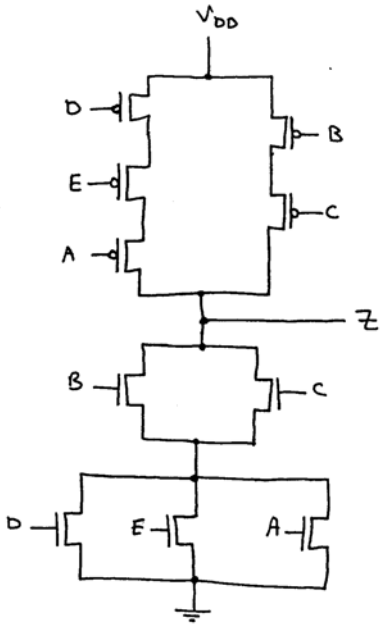


The equivalent inverter shown below has the following $\left(\frac{W}{L}\right)_{eq}$ ratio.

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_B} + \frac{1}{\left(\frac{W}{L}\right)_C}} + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_A} + \frac{1}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_E}}$$

Example

Find an equivalent CMOS inverter circuit for the following circuit for simultaneous switching of all inputs, assuming that $\left(\frac{W}{L}\right)_p = 15$ for all pMOS transistors and $\left(\frac{W}{L}\right)_n = 10$ for all nMOS transistors.



$$\left(\frac{W}{L}\right)_{n,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_E + \left(\frac{W}{L}\right)_A} + \frac{1}{\left(\frac{W}{L}\right)_B + \left(\frac{W}{L}\right)_C}}$$

$$= \frac{1}{\frac{1}{30} + \frac{1}{20}} = 12$$

$$\left(\frac{W}{L}\right)_{p,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_D} + \frac{1}{\left(\frac{W}{L}\right)_E} + \frac{1}{\left(\frac{W}{L}\right)_A}} + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_B} + \frac{1}{\left(\frac{W}{L}\right)_C}}$$

$$= \frac{1}{\frac{1}{15} + \frac{1}{15} + \frac{1}{15}} + \frac{1}{\frac{1}{15} + \frac{1}{15}} = 12.5$$

Thus, the equivalent CMOS inverter is shown below: