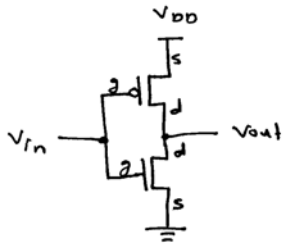
COE 360 Principles of VLSI Design
Dr. Aiman El-Maleh

Lecture#15

CMOS Inverter

COE 360 : Lec#15 Dr. Aiman EL-Malch

CMOS Inverter



- nmos transistor :
  - Conduction condition :

$$V_{gs} > V_{tn}$$

$$V_{in} > V_{tn}$$

  - Saturation condition :

$$V_{gd} \leq V_{tn}$$

$$V_{gs} - V_{ds} \leq V_{tn}$$

$$V_{in} - V_{out} \leq V_{tn}$$

$$V_{out} \geq V_{in} - V_{tn}$$

- pmos transistor :
  - Conduction condition :

$$V_{gs} < V_{tp}$$

$$V_{in} - V_{DD} < V_{tp}$$

  - Saturation condition :

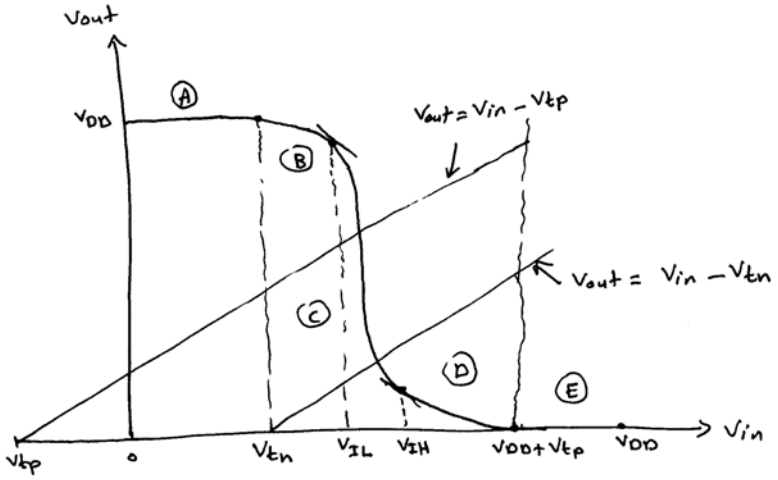
$$V_{gd} \geq V_{tp}$$

$$V_{gs} - V_{ds} \geq V_{tp}$$

$$(V_{in} - V_{DD}) - (V_{out} - V_{DD}) \geq V_{tp}$$

$$V_{in} - V_{out} \geq V_{tp}$$

$$V_{out} \leq V_{in} - V_{tp}$$



Region	Vin	Vout	nMOS	pMOS
A	$\leq V_{tn}$	V_{OH}	cutoff	linear
B	V_{IL}	high $\approx V_{OH}$	Saturation	linear
C	V_{th}	V_{th}	Saturation	Saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$\geq (V_{DD} + V_{tp})$	V_{OL}	linear	cutoff

In region A, where $V_{in} \leq V_{tn}$, the nMOS transistor is cutoff and the output voltage is equal to V_{OH}. As the input voltage is increased beyond V_{tn} (into region B),

the nMOS transistor starts conducting in saturation mode and the output voltage begins to decrease. Also note that the critical voltage V_{IL} which corresponds to $(dV_{out}/dV_{in}) = -1$ is located within Region B.

As the output voltage further decreases, the pMOS transistor enters saturation at the boundary of Region C. It can be seen from the figure that the inverter threshold voltage, where $V_{in} = V_{out}$, is located in Region C.

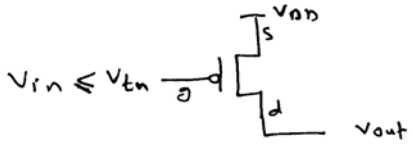
When the output voltage V_{out} falls below $(V_{in} - V_{tn})$, the nMOS transistor starts to operate in linear mode. This corresponds to Region D, where the critical voltage point V_{IH} with $(dV_{out}/dV_{in}) = -1$ is also located.

Finally, in Region E, with the input voltage $V_{in} \geq (V_{DD} + V_{tp})$, the pMOS transistor is cutoff, and the output voltage is V_{OL}.

Let us now calculate the critical voltage points on the VTC.

- Calculation of V_{OH}:

When $V_{in} \leq V_{tn}$, the nmos transistor is cutoff and we have the following situation:

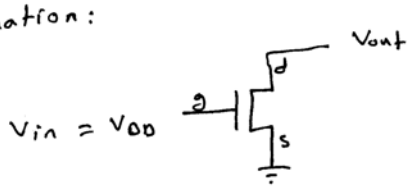


Since $V_{gs} = V_{tn} - V_{DD} < V_{tp}$, the pMos transistor will be conducting and $V_{out} = V_{DD}$.

Thus, $V_{OH} = V_{DD}$.

- Calculation of V_{OL}:

When $V_{in} = V_{OH} = V_{DD}$, the pmos transistor is cutoff and we have the following situation:



Since $V_{gs} = V_{in} = V_{DD} > V_{tn}$, the nmos transistor will be conducting and $V_{out} = 0$.

Thus, $V_{OL} = 0$.

Hence, the CMOS transistor produces a full swing between V_{DD} and 0. This implies that we will have good noise margins.

- Calculation of V_{IL}

By definition, the slope of the VTC is equal to (-1), i.e. $dV_{out}/dV_{in} = -1$ when the input voltage is $V_{in} = V_{IL}$. Note that in this case, the nMOS transistor operates in saturation while the pMOS transistor operates in the linear region. From $I_{D,n} = I_{D,p}$, we obtain the following current equation:

$$\frac{\beta_n}{2}\left(V_{gs,n} - V_{tn}\right)^2 = \frac{\beta_p}{2}\left[2\left(V_{gs,p} - V_{tp}\right)V_{DS,p} - V_{DS,p}^2\right]$$

$$\Rightarrow \frac{\beta_n}{2}\left(V_{in} - V_{tn}\right)^2 = \frac{\beta_p}{2}\left[2\left(V_{in} - V_{DD} - V_{tp}\right)\left(V_{out} - V_{DD}\right) - \left(V_{out} - V_{DD}\right)^2\right]$$

To satisfy the derivative condition at V_{IL}, we differentiate both sides with respect to V_{in}.

$$\beta_n\left(V_{in} - V_{tn}\right) = \beta_p\left[\left(V_{in} - V_{DD} - V_{tp}\right)\left(\frac{dV_{out}}{dV_{in}}\right) + \left(V_{out} - V_{DD}\right) - \left(V_{out} - V_{DD}\right)\left(\frac{dV_{out}}{dV_{in}}\right)\right]$$

Substituting $V_{in} = V_{IL}$ and $\frac{dV_{out}}{dV_{in}} = 1$, we obtain

$$\beta_n\left(V_{IL} - V_{tn}\right) = \beta_p\left(2V_{out} - V_{IL} + V_{tp} - V_{DD}\right)$$

$$\Rightarrow V_{IL} = \frac{2V_{out} + V_{tp} - V_{DD} + \frac{\beta_n}{\beta_p}V_{tn}}{1 + \frac{\beta_n}{\beta_p}}$$

This equation must be solved with the KCL equation to obtain the numerical value of V_{IL} and the corresponding output voltage V_{out}.

Calculation of V_{IH}

When the input voltage is equal to V_{IH}, the nMOS transistor operates in the linear region, and the pMOS transistor operates in saturation. Applying KCL to the output node, we obtain

$$\frac{\beta_n}{2}\left[2(V_{gs,n} - V_{tn})V_{ds,n} - V_{ds,n}^2\right] = \frac{\beta_p}{2}(V_{gs,p} - V_{tp})^2$$

$$\Rightarrow \frac{\beta_n}{2}\left[2(V_{in} - V_{tn})V_{out} - V_{out}^2\right] = \frac{\beta_p}{2}(V_{in} - V_{DD} - V_{tp})^2$$

Now differentiating both sides with respect to V_{in}, we obtain

$$\beta_n\left[(V_{in} - V_{tn})\left(\frac{dV_{out}}{dV_{in}}\right) + V_{out} - V_{out}\left(\frac{dV_{out}}{dV_{in}}\right)\right] = \beta_p(V_{in} - V_{DD} - V_{tp})$$

Substituting $V_{in} = V_{IH}$ and $(dV_{out}/dV_{in}) = -1$, we obtain:

$$\beta_n(-V_{IH} + V_{tn} + 2V_{out}) = \beta_p(V_{IH} - V_{DD} - V_{tp})$$

$$\Rightarrow V_{IH} = \frac{V_{DD} + V_{tp} + \frac{\beta_n}{\beta_p}(2V_{out} + V_{tn})}{1 + \frac{\beta_n}{\beta_p}}$$

Again, this equation must be solved simultaneously with the KCL equation to obtain the numerical values of V_{IH} and V_{out}.

- Calculation of V_{th}

The inverter threshold voltage is defined as $V_{th} = V_{in} = V_{out}$. Since the CMOS inverter exhibits large noise margins and a very sharp VTC transition, the inverter threshold voltage emerges as an important parameter characterizing the DC performance of the inverter.

For $V_{in} = V_{out}$, both transistors will be in saturation. So, we can write the KCL equation

$$\frac{\beta_n}{2}(V_{gs,n} - V_{tn})^2 = \frac{\beta_p}{2}(V_{gs,p} - V_{tp})^2$$

$$\Rightarrow \frac{\beta_n}{2}(V_{in} - V_{tn})^2 = \frac{\beta_p}{2}(V_{in} - V_{DD} - V_{tp})^2$$

This equation can be solved for the input voltage V_{in}:

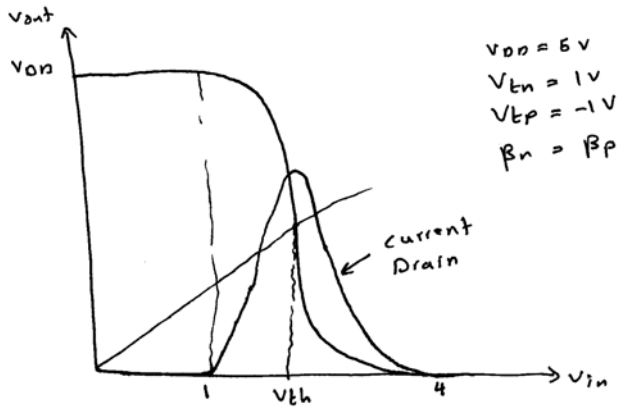
$$V_{in}\left[1 + \sqrt{\frac{\beta_p}{\beta_n}}\right] = V_{tn} + \sqrt{\frac{\beta_p}{\beta_n}}(V_{DD} + V_{tp})$$

* Note here that when we take the square root there are two solutions ±. we pick here the -ve.

Finally, the inverter threshold (switching threshold) voltage V_{th} is found as

$$V_{th} = \frac{V_{tn} + \sqrt{\frac{\beta_p}{\beta_n}}\,(V_{DD} + V_{tp})}{\left(1 + \sqrt{\frac{\beta_p}{\beta_n}}\right)}$$

Note that the inverter threshold voltage is defined as $V_{th} = V_{in} = V_{out}$. When the input voltage $V_{in} = V_{th}$, the current being drawn from the power source during transition reaches its peak.



Design of CMOS inverters

The CMOS inverter provides a full output voltage swing between 0 and V_{DD} and therefore, the noise margins are relatively wide.

Thus, the problem of designing a CMOS inverter can be reduced to setting the inverter threshold to a desired value.

Given the power supply voltage V_{DD}, the nMOS and the pMOS transistor threshold voltages, and the desired inverter threshold voltage V_{th}, the corresponding ratio $\frac{\beta_p}{\beta_n}$ can be found as follows:

$$\sqrt{\frac{\beta_p}{\beta_n}} = \frac{V_{th} - V_{tn}}{V_{DD} + V_{tp} - V_{th}}$$

$$\text{Thus, } \frac{\beta_n}{\beta_p} = \left(\frac{V_{DD} + V_{tp} - V_{th}}{V_{th} - V_{tn}} \right)^2$$

Now, recall that the switching threshold voltage of an ideal inverter is defined as

$$V_{th,ideal} = \frac{1}{2} V_{DD}$$

Substituting this in the above equation:

$$\Rightarrow \left(\frac{\beta_n}{\beta_p}\right)_{ideal} = \left(\frac{0.5 V_{DD} + V_{tp}}{0.5 V_{DD} - V_{tn}} \right)^2$$

Since the operations of the nMOS and the pMOS transistors of the CMOS inverter are fully complementary, we can achieve completely symmetric input-output characteristics by setting the threshold voltages as $V_{tn} = |V_{tp}|$.

This implies that $\left(\frac{\beta_n}{\beta_p}\right)_{\substack{\text{symmetric}\\ \text{inverter}}} = 1$

Note that $\frac{\beta_n}{\beta_p} = \frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p} = \frac{\mu_n \left(\frac{W}{L}\right)_n}{\mu_p \left(\frac{W}{L}\right)_p}$

assuming that the gate oxide thickness t_{ox}, and hence the gate oxide capacitance C_{ox} have the same value for both nMOS and pMOS transistors.

The unity-ratio condition $\frac{\beta_n}{\beta_p} = 1$ for the ideal symmetric inverter requires that

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n}$$

Typically, $\mu_n \simeq 2.5\, \mu_p$

Hence, $\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n * 2.5$

For a symmetric CMOS inverter with $V_{tn} = V_{tp}$ and $\frac{\beta_n}{\beta_p} = 1$, V_{IL} can be reduced to

$$V_{IL} = \frac{1}{8}\left(3 V_{DD} + 2 V_{tn}\right)$$

Also, V_{IH} can be reduced to

$$V_{IH} = \frac{1}{8}\left(5 V_{DD} - 2 V_{tn}\right)$$

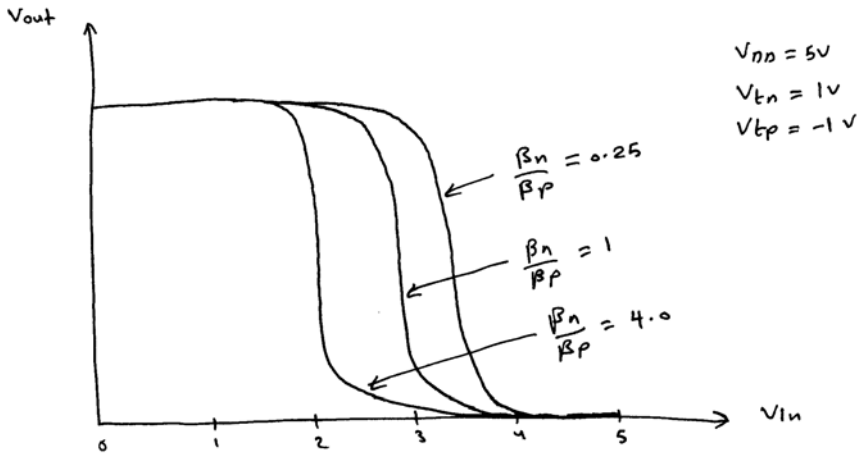
Note that the sum of V_{IL} and V_{IH} is always equal to V_{DD} in a symmetric inverter : $V_{IL} + V_{IH} = V_{DD}$

The noise margins for a symmetric inverter are as follows:

$$NM_L = V_{IL} - V_{OL} = V_{IL}$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH} = V_{IL}$$

Thus, $NM_L = NM_H = V_{IL}$



Power Dissipation

Since the CMOS inverter does not draw any significant current from the power supply in both of its steady state points ($V_{out} = V_{OH}$ and $V_{out} = V_{OL}$), the DC power dissipation of this circuit is almost negligible.

Example

Consider a CMOS inverter with the following parameters:

$V_{DD} = 5V$, $V_{tn} = 1V$, $V_{tp} = -1.2V$,

$\beta_n = 100\ \mu A/V^2$, $\beta_p = 40\ \mu A/V^2$

Calculate the noise margins of the circuit.

Solution

Notice that the CMOS inverter being considered here has $\frac{\beta_n}{\beta_p} = 2.5$ and $V_{tn} \neq |V_{tp}|$. Hence, it is not symmetric.

First, $V_{OH} = 5V$ and $V_{OL} = 0V$.

$$V_{IL} = \frac{2V_{out} + V_{tp} - V_{DD} + \frac{\beta_n}{\beta_p} V_{tn}}{1 + \frac{\beta_n}{\beta_p}}$$

$$= \frac{2V_{out} - 1.2 - 5 + 2.5}{1 + 2.5} = 0.57\,V_{out} - 1.06$$

Now substituting this in the KCL equation:

$$2.5\,(0.57\,V_{out} - 1.06 - 1)^2 = 2\,(0.57\,V_{out} - 1.06 - 5 + 1.2)(V_{out} - 5) - (V_{out} - 5)^2$$

This expression yields a second-order polynomial as follows:

$$0.66\,V_{out}^2 - 0.46\,V_{out} - 13 = 0$$

Only one root of this quadratic equation corresponds to a physically correct solution for V_{out} (i.e. $V_{out} > 0$)

$\Rightarrow V_{out} = 4.8\ V$

From this value, we can calculate the critical voltage V_{IL} as:

$$V_{IL} = (0.57)(4.8) - 1.06 = \underline{\underline{1.68\ V}}$$

To calculate V_{IH} in terms of the output voltage

$$V_{IH} = \frac{V_{DD} + V_{tp} + \frac{\beta_n}{\beta_p}(2V_{out} + V_{tn})}{1 + \frac{\beta_n}{\beta_p}}$$

$$= \frac{5 - 1.2 + 2.5(2V_{out} + 1)}{1 + 2.5} = 1.43\,V_{out} + 1.8$$

Next, we substitute this in the KCL equation:

$$2.5\left[2(1.43\,V_{out} + 1.8 - 1)V_{out} - V_{out}^2\right] = (1.43V_{out} - 2)^2$$

$$\Rightarrow 2.61\,V_{out}^2 + 9.72\,V_{out} - 4 = 0$$

Again, only one root of this quadratic equation corresponds to the physically correct solution for V_{out} when $V_{in} = V_{IH}$

$$V_{out} = 0.37\ V \Rightarrow V_{IH} = (1.43)(0.37) + 1.8$$
$$= \underline{\underline{2.33\ V}}$$

Thus, $NM_L = V_{IL} - V_{OL} = 1.68\ V$

$NM_H = V_{OH} - V_{IH} = 5 - 2.33 = \underline{\underline{2.67\ V}}$