

**COE 360 Principles of VLSI Design**  
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**Lecture#13**

**Inverter with Enhancement-Type MOSFET  
Load**

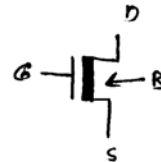
Inverter with Enhancement-type MOSFET Load

- Resistive-load inverters are not suitable candidates for most VLSI system applications primarily because of the large area occupied by the load resistor
- Mos transistors can be used as active load devices with less area and better performance
- There are two types of nMOS transistors:

- Enhancement-type: This is the regular known type where  $V_t > 0$  and the transistor conducts when  $V_{gs} \geq V_t$ .



- Depletion-type: Using selective ion implantation into the channel, the threshold voltage of an n-channel can be made negative. This means that the resulting nMOS transistor will have a conducting channel at  $V_{gs} = 0$ , enabling current flow between its source and drain as long as  $V_{gs}$  is larger than the negative threshold voltage. Such a device is called a depletion-type (or normally-on) n-channel MOS.



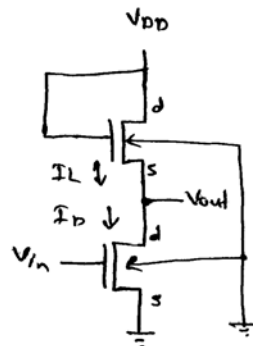
- An enhancement-type nMOS transistor can be used as an active load device operating either in saturation or linear region. This depends on the bias voltage applied to its gate. Thus, we have two different types of inverters with an enhancement load.

### Saturated Enhancement-Load Inverter

Since  $V_{SB, driver} = 0$ , then

$$V_{T, driver} = V_{T0}$$

However, since  $V_{SB, load} > 0$ ,  $V_{T, load}$  is a function of the source-to-substrate voltage due to bias effect.



First, let us consider the operating region of the load device.

Since both the gate and drain of the load transistor are connected to  $V_{DD}$ , we have

$$V_{GS, load} = V_{DS, load}. \text{ Thus, } V_{GS, load} = 0 < V_{T, load}.$$

Hence, the load transistor operates in saturation as long as it is on, i.e.

$$V_{GS, load} \geq V_{T, load}.$$

The load current can be expressed as:

$$I_{D, load} = \frac{\beta_{load}}{2} [V_{GS, load} - V_{T, load}]^2$$

Next, let us briefly examine the critical voltage points which characterize the VTC of this inverter.

### Calculation of $V_{OH}$

When  $V_{in} < V_{T0}$ , the driver transistor is cutoff.  $I_D = I_L = 0$ .

Since the load transistor is on as long as

$V_{GS,load} \geq V_{T,load}$ , we can find  $V_{OH}$  by

solving  $V_{GS,load} = V_{DD} - V_{out} = V_{T,load}$

$$\begin{aligned} V_{OH} &= V_{DD} - V_{T,load}(V_{OH}) \\ &= V_{DD} - \left[ V_{T0} + \gamma \left( \sqrt{|2\phi_f| + V_{OH}} - \sqrt{|2\phi_f|} \right) \right] \end{aligned}$$

$$\Rightarrow V_{OH} - V_{DD} + V_{T0} - \gamma \sqrt{|2\phi_f|} = -\gamma \sqrt{|2\phi_f| + V_{OH}}$$

Squaring both sides:

$$\Rightarrow \left[ V_{OH} - (V_{DD} - V_{T0} + \gamma \sqrt{|2\phi_f|}) \right]^2 = \left[ -\gamma \sqrt{|2\phi_f| + V_{OH}} \right]^2$$

$$\begin{aligned} \Rightarrow V_{OH}^2 - 2 \left[ V_{DD} - V_{T0} + \gamma \sqrt{|2\phi_f|} \right] V_{OH} \\ + \left[ V_{DD} - V_{T0} + \gamma \sqrt{|2\phi_f|} \right]^2 = \gamma^2 |2\phi_f| + \gamma^2 V_{OH} \end{aligned}$$

$$\begin{aligned} \Rightarrow V_{OH}^2 - \left[ 2(V_{DD} - V_{T0} + \gamma \sqrt{|2\phi_f|}) + \gamma^2 \right] V_{OH} \\ + \left[ (V_{DD} - V_{T0} + \gamma \sqrt{|2\phi_f|})^2 - \gamma^2 |2\phi_f| \right] = 0 \end{aligned}$$

The solution of this quadratic equation yields the output high voltage  $V_{OH}$ . Note here that the output voltage cannot exceed  $V_{DD} - V_{T,load}$ , a limitation which significantly reduces the noise margin  $NMH$ .

### Calculation of $V_{OL}$

For calculating  $V_{OL}$ , we assume that  $V_{in} = V_{OH}$ .

Since  $V_{gs} = V_{OH} - V_{OL} > V_{T0}$ , the driver transistor operates in the linear region.

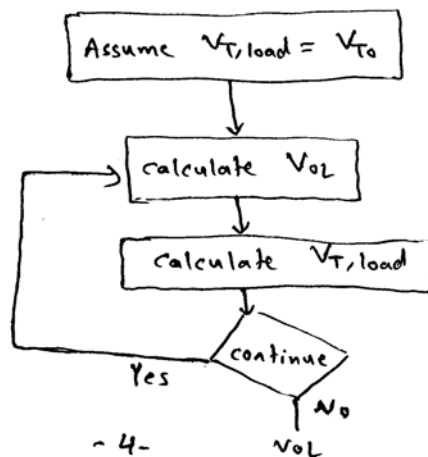
Using KCL,  $I_L = I_D$

$$\begin{aligned} \Rightarrow \frac{\beta_{load}}{2} [V_{DD} - V_{OL} - V_{T,load}(V_{OL})]^2 \\ = \frac{\beta_{driver}}{2} [2(V_{OH} - V_{T0})V_{OL} - V_{OL}^2] \end{aligned}$$

The value of  $V_{OH}$  must be found first using the previous analysis. Also, note here that the threshold voltage of the load transistor  $V_{T,load}$  is a function of  $V_{OL}$  as follows

$$V_{T,load} = V_{T0} + \gamma \left[ \sqrt{|2\phi_F| + V_{OL}} - \sqrt{|2\phi_F|} \right]$$

To find  $V_{OL}$ , we need to solve these two equations. Alternatively,  $V_{OL}$  can be calculated through a simple technique based on numerical iteration, as follows.



Initially, we assume  $V_{T,load} = V_{T0}$  and calculate the value of  $V_{OL}$ . Then, we use this value to find a better estimate for  $V_{T,load}$ . The computed threshold value is then used to obtain a more accurate estimate for  $V_{OL}$ . This cycle can be repeated several times, until subsequent iterations do not cause a significant change in  $V_{OL}$ .

\* Calculation of  $V_{IL}$

At  $V_{in} = V_{IL}$ , the output voltage is expected to be very close to  $V_{OH}$ . Since  $V_{IL} > V_{T0}$ , the driver transistor will be turned on and will operate in the saturation region since  $V_{gd} = V_{IL} - V_{out} < V_{T0}$ .

Thus, by KCL

$$\frac{\beta_{load}}{2} (V_{DD} - V_{out} - V_{T,load})^2 = \frac{\beta_{driver}}{2} (V_{in} - V_{T0})^2$$

Also, we know that  $\frac{dV_{out}}{dV_{in}} = -1$

Differentiating both sides with respect to  $V_{in}$ :

$$\beta_{load} (V_{DD} - V_{out} - V_{T,load}) \cdot \left[ -\frac{dV_{out}}{dV_{in}} - \frac{dV_{T,load}}{dV_{out}} \cdot \frac{dV_{out}}{dV_{in}} \right] = \beta_{driver} (V_{in} - V_{T0})$$

This equation can be rewritten as follows:

$$\frac{dV_{out}}{dV_{in}} = - \frac{\beta_{driver} (V_{in} - V_{to})}{\left(1 + \frac{dV_{T,load}}{dV_{out}}\right) \beta_{load} (V_{DD} - V_{out} - V_{T,load})}$$

Assuming that  $\frac{dV_{T,load}}{dV_{out}}$  is negligible compared to 1, we obtain the following relationship:

$$\frac{dV_{out}}{dV_{in}} = - \frac{\sqrt{2 \beta_{driver} \cdot I_{D,driver}}}{\sqrt{2 \beta_{load} \cdot I_{D,load}}}$$

Since  $I_{D,load} = I_{D,driver}$ , this equation

yields 
$$\frac{dV_{out}}{dV_{in}} = - \sqrt{\frac{\beta_{driver}}{\beta_{load}}}$$

This result implies that the slope of the VTC will be equal to a negative constant, determined by the transconductances of the driver and the load devices, after the driver is turned on and as long as both devices are in saturation.

Hence, in this case  $V_{IL}$  is not defined as the point at which the slope of the VTC is equal to zero. For practical purposes  $V_{IL} = V_{to}$ .

\* Calculation of  $V_{IH}$

When  $V_{in} = V_{IH}$ , the output voltage  $V_{out}$  is expected to be slightly larger than  $V_{OL}$ . Assuming that  $V_{out} < V_{IH} - V_{to}$ , the driver transistor operates in the linear region, while the load transistor is still in saturation.

$$\frac{\beta_{load}}{2} (V_{DD} - V_{out} - V_{T,load})^2 = \frac{\beta_{driver}}{2} [2(V_{in} - V_{to}) \cdot V_{out} - V_{out}^2]$$

Also, since  $\frac{dV_{out}}{dV_{in}} = -1$ , we differentiate both sides with respect to  $V_{in}$ :

$$\beta_{load} (V_{DD} - V_{out} - V_{T,load}) \left[ -\frac{dV_{out}}{dV_{in}} - \frac{dV_{T,load}}{dV_{out}} \cdot \frac{dV_{out}}{dV_{in}} \right]$$

$$= \beta_{driver} \left[ 2(V_{in} - V_{to}) \frac{dV_{out}}{dV_{in}} + 2V_{out} - 2V_{out} \frac{dV_{out}}{dV_{in}} \right]$$

Substituting  $\frac{dV_{out}}{dV_{in}} = -1$  and assuming that  $\frac{dV_{T,load}}{dV_{out}}$  is negligible compared to 1, we obtain

$$\beta_{load} (V_{DD} - V_{out} - V_{T,load}) = \beta_{driver} [2V_{out} - V_{in} + V_{to}]$$

$$\Rightarrow V_{IH} = V_{to} - \frac{\beta_{load}}{\beta_{driver}} [V_{DD} - V_{T,load}] + \left[ 2 + \frac{\beta_{load}}{\beta_{driver}} \right] V_{OL}$$



Now, substituting this equation in the KCL equation and solving for  $V_{out}$ , we obtain

$$\left[ (V_{DD} - V_{T,load}) - V_{out} \right]^2 = \frac{\beta_{driver}}{\beta_{load}} \left[ 2 \left[ V_{to} - \frac{\beta_{load}}{\beta_{driver}} (V_{DD} - V_{T,load}) + \left( 2 + \frac{\beta_{load}}{\beta_{driver}} \right) V_{out} - V_{to} \right] V_{out} - V_{out}^2 \right]$$

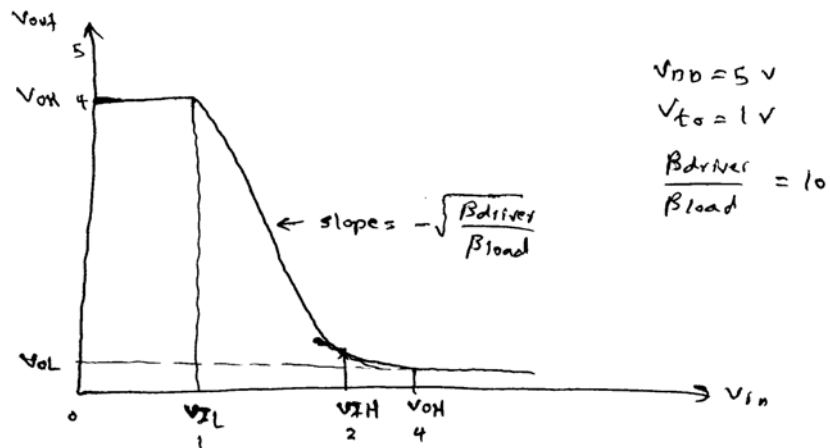
$$\begin{aligned} \Rightarrow (V_{DD} - V_{T,load})^2 - 2(V_{DD} - V_{T,load})V_{out} + V_{out}^2 \\ = -2(V_{DD} - V_{T,load})V_{out} + 4 \frac{\beta_{driver}}{\beta_{load}} V_{out}^2 \\ + 2V_{out}^2 - \frac{\beta_{driver}}{\beta_{load}} V_{out}^2 \end{aligned}$$

$$\Rightarrow (V_{DD} - V_{T,load})^2 = \left[ 1 + \frac{3\beta_{driver}}{\beta_{load}} \right] V_{out}^2$$

$$\Rightarrow V_{out} = \sqrt{\frac{\beta_{load}}{\beta_{load} + 3\beta_{driver}}} (V_{DD} - V_{T,load})$$

Note that the threshold voltage of the load device is also a function of the output voltage.

The typical DC voltage transfer characteristic (VTC) of the saturated enhancement-load inverter is shown below:



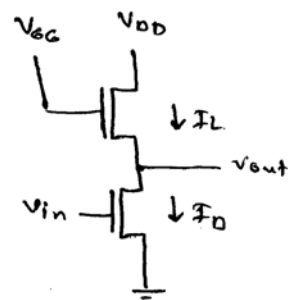
Obviously, the most significant performance deficiency of this circuit is that the output high voltage  $V_{OH}$  is lower than the power supply voltage  $V_{DD}$ , i.e.  $V_{OH} = V_{DD} - V_{T,load}$ . Thus, the noise margin for high signal levels (NMH) is greatly reduced for this inverter.

## Linear Enhancement-Load Inverter

We saw that the most significant problem with the saturated enhancement-load inverter is that the output voltage  $V_{OH}$  is lower than the supply voltage  $V_{DD}$ .

One possible solution to this problem is to apply the gate bias of the enhancement-type load device from another voltage source  $V_{GG}$ , so that the load device operates in the linear region instead of the saturation region, as shown below.

To ensure that the load transistor operates in the linear region regardless of input and output voltage levels, we must set the gate bias voltage as  $V_{GG} > V_{DD} + V_{T,load}$ .



When  $V_{in} = \text{low}$ , the output voltage reaches  $V_{OH} = V_{DD}$ . Hence, this circuit does not suffer from the limitations imposed on the noise margin  $NM_H$  by the lower  $V_{OH}$  value. The price of this improvement is paid, however, by using two separate power supplies,  $V_{DD}$  and  $V_{GG}$ .

To supply each circuit designed in this fashion with three power connections (two for supply voltages, one ground) is costly in terms of area and routing requirements. This circuit is not widely used in large-scale applications.

Both the saturated and the linear enhancement-load inverter circuits require a relatively large driver-to-load ratio,  $\beta_D/\beta_L$ , to achieve a sharp VTC transition, lower  $V_{OL}$ , and larger noise margins.

A larger driver-to-load ratio, on the other hand, increases the total area occupied by the inverter circuit and, hence, is not well-suited for large scale integration.