COE 360 HW#6 Dr. Aiman El-Maleh

Q1 $T_{ox} = 120 \times 10^{-8}$ cm

$\varepsilon_o \varepsilon_{sio2} = 3.9 \times 8.854 \times 10^{-14}$ F/cm

$$C_{ox} = \frac{\varepsilon_o \varepsilon_{sio2}}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-14}}{120 \times 10^{-8}} \text{ F/cm}$$

$= 0.288 \times 10^{-6}$ F/cm^2

$= 0.288 \times 10^{-6}$ F/10^8 μm^2

$= 0.288 \times 10^{-14}$ F/μm^2

$= 28.8 \times 10^{-4}$ pF/μm^2

C_g (intrinsic) $= W \times L \times C_{ox}$

$= 4 \times 1 \times 28.8 \times 10^{-4}$ pF

$= 0.0115$ pF

C_g (extrinsic) $= (W \times C_{gso}) + (W \times C_{gdo}) + (2L \times C_{gbo})$

$= (4 \times 6 \times 10^{-4}) + (4 \times 6 \times 10^{-4}) + (2 \times 1 \times 2 \times 10^{-4})$ pF

$= 0.0052$ pF

Thus, $C_g = C_g$ (intrinsic) $+ C_g$ (extrinsic)

$= 0.0115 + 0.0052$

$= \underline{\underline{0.0167}}$ pF

$$C_j = \left(\text{Area} \times C_J \times \left(1 + \frac{V_J}{PB} \right)^{-MJ} \right) + \left(\text{periphery} \times C_{JSW} \times \left(1 + \frac{V_J}{PB} \right)^{-MJSW} \right)$$

$A_S = AD = 15 \times 10^{-12} \ m^2$

$P_S = PD = 10 \times 10^{-6} \ m$

$c_J = 200 \times 10^{-12} \ F/m^2$

$C_{JSW} = 400 \times 10^{-12} \ F/m^2$

$V_{sb} = 0$, $V_{db} = 2.5$, $PB = 0.6$

$MJ = 0.5$, $MJSW = 0.3$

$$C_{jsource} = \left(15 \times 10^{-12} \times 200 \times 10^{-12} \times \left(1 + \frac{0}{0.6} \right)^{-0.5} \right) + \left(10 \times 10^{-6} \times 400 \times 10^{-12} \times \left(1 + \frac{0}{0.6} \right)^{-0.3} \right)$$

$$= 30 \times 10^{-22} + 4 \times 10^{-15}$$

$$= \underline{0.004} \ pF$$

$$C_{jdrain} = \left(15 \times 10^{-12} \times 200 \times 10^{-12} \times \left(1 + \frac{2.5}{0.6} \right)^{-0.5} \right) + \left(10 \times 10^{-6} \times 400 \times 10^{-12} \times \left(1 + \frac{2.5}{0.6} \right)^{-0.3} \right)$$

$$= 30 \times 10^{-22} \times 0.44 + 4 \times 10^{-15} \times 0.61$$

$$= \underline{0.00244} \ pF$$

Notice that the drain capacitance is smaller than the source capacitance because the junction is reverse biased, which increases the size of the depletion region.

Q2

(i) The parasitics are as follows:

$$C_{m1} = 15 \times 30 \times 10^{-18} = 450 \times 10^{-18} \text{ F}$$

$$C_p = 10 \times 50 \times 10^{-18} = 500 \times 10^{-18} \text{ F}$$

$$C_g = 8 \times 1800 \times 10^{-18} = 14400 \times 10^{-18} \text{ F}$$

$$C_{cell} = 450 \times 10^{-18} + 500 \times 10^{-18} + 14400 \times 10^{-18}$$

$$= 0.015 \text{ pF}$$

$$C_{32\text{-cell}} = 32 \times C_{cell} = 32 \times 0.015 = 0.49 \text{ pF}$$

(ii) $R_{silicide} = 2000 \times 4 = 8000 \ \Omega$

$$C_{silicide} = 2000 \times 20 \times 10^{-18} = 0.04 \text{ pF}$$

$$C_{total} = 0.49 + 0.04 = 0.53 \text{ pF}$$

$$RC = 8000 \times 0.53 \times 10^{-12}$$

$$= 4.24 \text{ ns}$$

(iii) Note that $RC = \frac{L}{W} R_s \left(C_{32\text{-cell}} + L.W. C_{silicide} \right)$

$$= \frac{L}{W} R_s C_{32\text{-cell}} + L^2 C_{silicide}$$

$$\Rightarrow W = \frac{L R_s C_{32\text{-cell}}}{RC - L^2 C_{silicide}}$$

$$\Rightarrow \frac{W_2}{W_1} = \frac{(RC)_1 - L^2 C_{silicide}}{(RC)_2 - L^2 C_{silicide}} \simeq \frac{(Rc)_1}{(Rc)_2}$$

Thus, $W_2 = W_1 \times \frac{(Rc)_1}{(Rc)_2}$

$= 1\,\mu m \times \frac{4.24}{2} = 2.12\,\mu m$

Thus, we say that the width has to be $2.12\,\mu m$.

To verify our answer, we recalculate the RC delay with this width.

$R_{sili} = \frac{2000}{2.12} \times 4 = 3773.58\,\Omega$

$C_{sili} = \frac{2000}{2.12} \times 20 \times 10^{-18} = 0.0189\ pF$

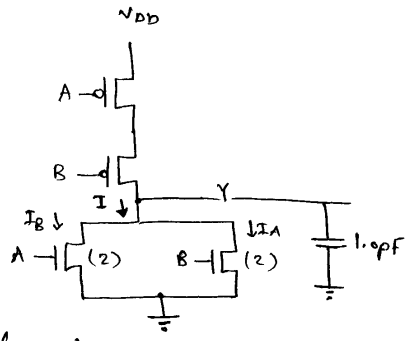
$C_{total} = 0.49 + 0.0189 = 0.509\ pF$

$RC = 3773.58 \times 0.509 \times 10^{-12}$

$= \underline{\underline{1.92}}\ ns$

Q3 $Y = (A + B)'$

- When $V_A = 5\,V$, $I_A = 2\,mA$ (sat.) for $V_y \geq 4.0\,V$
- When $V_B = 5\,V$, $I_B = 2\,mA$ (sat.) for $V_y \geq 4.0\,V$



We can deduce from this information that $V_{T,A} = V_{T,B} = 1.0\,V$ since the nmos transistor enters saturation when $V_{DS} \geq V_{GS} - V_T$

V_A and V_B are equal to 5 V for $t \geq 0$

The current equation when the drivers are in saturation is:

$$C\frac{dV_y}{dt} = -I_{sat} = -\frac{1}{2}\beta_n (V_{OH} - V_{T,n})^2$$

We can calculate the time in which the nMOS transistor operates in saturation by integrating the above equation

$$\int_{t=0}^{t=t_{sat}} dt = -\int_{V_y=5}^{V_y=4.0} \frac{C\,dV_y}{I_{sat}}$$

$$t_{sat} = \frac{-C}{I_{sat}} \left[V_y \right]_5^{4.0} = \frac{-C}{I_{sat}} \left[-1.0 \right]$$

$$= \frac{(1.0V)(1pF)}{4\ mA} = 0.25ns$$

$$\beta_n = \frac{2\ I_{sat}}{(V_{OH} - V_{Tn})^2} = \frac{(2)(4mA)}{(4.0)^2} = 0.5 \times 10^{-3}\ A/V^2$$

The current equation for the linear operating region is written as

$$C\frac{dv_{out}}{dt} = -I = -\frac{1}{2}\beta_n \left[2(V_{OH} - V_{Tn})Y - Y^2 \right]$$

Integrating this differential equation between the two voltage boundary conditions yields the amount of time in which the nMOS transistor operates in the linear region.

$$\int_{t=t_{sat}}^{t=t_{delay}} dt = \frac{-2C}{\beta_n} \int_{y=4.0}^{y=2.5} \frac{dy}{\left[2(V_{OH} - V_{Tn})Y - Y^2 \right]}$$

$$t_{delay} - t_{sat} = \frac{-2C}{\beta_n} \int_{4.0}^{2.5} \frac{dy}{8.0y - y^2}$$

$$\int \frac{dy}{8.4y - y^2} = \int \frac{dy}{(8.0-y)\,y} = \int dy \left\{ \frac{A}{y} + \frac{B}{8.4-y} \right\}$$

$$\Rightarrow \frac{A}{y} + \frac{B}{8.0-y} = \frac{A(8.0-y) + By}{(8.0-y)\,y} = \frac{1}{(8.0y-y)\,y}$$

$$\Rightarrow A = \frac{1}{8.0} \qquad B - A = 0 \Rightarrow B = A = \frac{1}{8.0}$$

$$\Rightarrow \frac{-2C}{\beta_n} \int_{4.0}^{2.5} \frac{dy}{8.4y - y^2} = \frac{-2C}{\beta_n} \cdot \frac{1}{8.0} \int_{4.0}^{2.5} \left\{ \frac{1}{y} + \frac{1}{8.0-y} \right\} dy$$

$$\Rightarrow = \frac{-2C}{\beta_n} \cdot \frac{1}{8.0} \ln\left(\frac{y}{8.0-y} \right) \Big|_{4.0}^{2.5}$$

$$= \frac{-2 * 1 \times 10^{-12}}{0.5 \times 10^{-3} \times 8.0} \left[\ln \frac{2.5}{5.5} - \ln \frac{4.0}{4.0} \right]$$

$$= \frac{2 \times 1 \times 10^{-12} \times 0.79}{0.5 \times 10^{-3} \times 8.0} = 0.39 \text{ ns}$$

Thus, the total delay $t_{delay} = 0.25 + 0.39 = 0.64 \text{ns}$

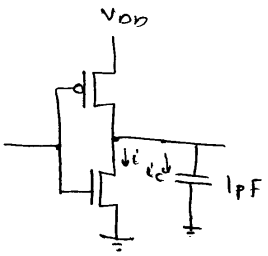
We know that the delay can be expressed as follows $t_{delay} = K \frac{C_L}{\beta_n}$, where K is a constant.

$$\frac{(t_{delay})_2}{(t_{delay})_1} = \frac{\frac{K C_L}{\beta_{n2}}}{\frac{K C_L}{\beta_{n1}}} = \frac{\beta_{n1}}{\beta_{n2}} = \frac{\mu C_{ox} \left(\frac{W}{L}\right)_1}{\mu C_{ox} \left(\frac{W}{L}\right)_2}$$

$$\Rightarrow (t_{delay})_2 = (t_{delay})_1 * \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}$$

$$= 0.64 \text{ ns} * \frac{2}{4} = \underline{0.32} \text{ ns}$$

Q4 We solve the problem for a CMOS inverter, and then design the 2-input NAND and NOR gates.



$t_{falling} = t_{V_{10\%}} - t_{V_{90\%}}$

$V_{10\%} = 0.5$

$V_{90\%} = 4.5$

$t_{falling}$ can then be found as follows:

$$t_{falling} = \int_{t_{V=4.5}}^{t_{V=4}} dt + \int_{t_{V=4}}^{t_{V=0.5}} dt$$

$$i_C = -i$$

$$C \frac{d\,v_{out}}{dt} = -i$$

$$\int_{t_{V=4.5}}^{t_{V=4}} dt = -C \int_{4.5}^{4} \frac{d\,v_{out}}{i} = -C \int_{4.5}^{4} \frac{d\,v_{out}}{\frac{\beta_n}{2}(V_{OH} - V_{tn})^2}$$

$$= \frac{-2C}{\beta_n (V_{OH} - V_{tn})^2} \left[4 - 4.5 \right]$$

$$= \frac{-2 \times 1 \times 10^{-12} \times -0.5}{\beta_n \times 16} = \frac{1 \times 10^{-12}}{16 \times \beta_n}$$

$$\int_{tv=4}^{tv=0.5} dt = -C \int_{4}^{0.5} \frac{d\,vout}{i} = -C \int_{4}^{0.5} \frac{d\,vout}{\frac{\beta n}{2}\left[2(VoH-Vt)\,Vout - Vout^2\right]}$$

$$= \frac{-2C}{\beta n} \int_{4}^{0.5} \frac{d\,vout}{8\,Vout - Vout^2}$$

$$\int \frac{d\,vout}{8\,Vout - Vout^2} = \int \frac{d\,vout}{(8 - Vout)\,Vout} = \int \left\{\frac{A}{Vout} + \frac{B}{8 - Vout}\right] dv_o$$

$$\frac{1}{(8 - Vout)\,Vout} = \frac{A}{Vout} + \frac{B}{8 - Vout} = \frac{A(8 - Vout) + B\,Vout}{(8 - Vout)\,Vout}$$

$$\Rightarrow \quad A = \frac{1}{8} \quad , \quad B = \frac{1}{8}$$

$$\Rightarrow \int \frac{d\,vout}{8\,Vout - Vout^2} = \frac{1}{8} \int \frac{d\,vout}{Vout} + \frac{1}{8} \int \frac{d\,vout}{8 - Vout}$$

$$= \frac{1}{8} \ln \frac{Vout}{8 - Vout}$$

$$\Rightarrow \int_{tv=4}^{tv=0.5} dt = \frac{2C}{\beta n} \cdot \frac{1}{8} \left[\ln \frac{8 - Vout}{Vout}\right]_{4}^{0.5}$$

$$= \frac{2C}{\beta n} \cdot \frac{1}{8} \left\{2.71\right] = \frac{1 \times 10^{-12} \times 2.71}{\beta n\ 4}$$

Thus, $t_{falling} = \frac{1 \times 10^{-12}}{16 \beta_n} + \frac{1 \times 10^{-12}}{4 \beta_n} \times 2.71 = 2ns$

$$= \frac{0.741 \times 10^{-12}}{\beta_n} = 2ns$$

$$\Rightarrow \beta_n = \frac{0.741 \times 10^{-12}}{2 \times 10^{-9}} = 0.37 \times 10^{-3}$$

$$\Rightarrow \left(\frac{W}{L}\right)_n = \frac{0.37 \times 10^{-3}}{100 \times 10^{-6}} = \underline{\underline{3.7}}$$

For a CMOS inverter, we know that the inverter threshold is as follows:

$$V_{th} = \frac{V_{tn} + \sqrt{\frac{\beta_p}{\beta_n}} (V_{DD} + V_{tp})}{1 + \sqrt{\frac{\beta_p}{\beta_n}}}$$

$$\Rightarrow 2.5 = \frac{1 + \sqrt{\frac{\beta_p}{\beta_n}} (5 - 0.8)}{1 + \sqrt{\frac{\beta_p}{\beta_n}}}$$

$$\Rightarrow 2.5 + 2.5\sqrt{\frac{\beta_p}{\beta_n}} = 1 + 4.2\sqrt{\frac{\beta_p}{\beta_n}}$$

$$\Rightarrow 1.7\sqrt{\frac{\beta_p}{\beta_n}} = 1.5$$

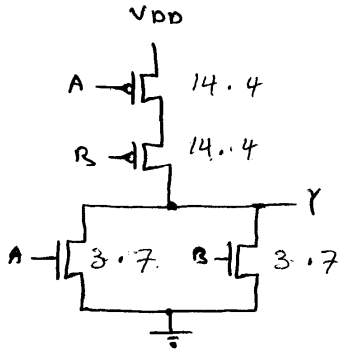
$$\Rightarrow \sqrt{\frac{\beta_p}{\beta_n}} = \frac{1.5}{1.7} = 0.88 \Rightarrow \frac{\beta_p}{\beta_n} = 0.779$$

$$\frac{\beta_p}{\beta_n} = \frac{\mu_p \; C_{ox} \; \left(\frac{W}{L}\right)_p}{\mu_n \; C_{ox} \; \left(\frac{W}{L}\right)_n}$$

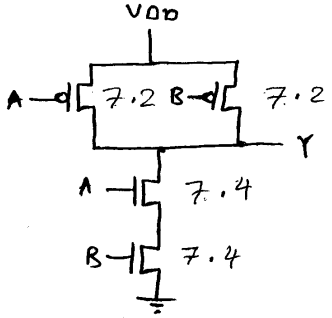
$$\Rightarrow \left(\frac{W}{L}\right)_p = \frac{\beta_p}{\beta_n} \times \frac{\mu_n \; C_{ox} \left(\frac{W}{L}\right)_n}{\mu_p \; C_{ox}}$$

$$= 0.779 \times \frac{100 \times 10^{-6}}{40 \times 10^{-6}} \times 3.7 = \underline{\underline{7.2}}$$

Thus, the 2-input NOR gate is designed as follows:



The 2-input NAND gate is designed as follows:



(ii) For a CMOS inverter, the rising time can be derived in a similar approach to what we used for deriving the falling time. We can use the equation given in the book.

$$t_r = \frac{2 C_L}{\beta_p V_{DD} (1-p)} \left[\frac{(p-0.1)}{(1-p)} + \frac{1}{2} \ln (19 - 20p) \right]$$

where $p = |V_{tp}| / V_{DD}$

$$\Rightarrow t_r = \frac{2 \times 1 \times 10^{-12}}{\beta_p \times 5 (1 - \frac{0.8}{5})} \left[\frac{(\frac{0.8}{5} - 0.1)}{(1 - \frac{0.8}{5})} + \frac{1}{2} \ln (19 - 20 \times \frac{0.8}{5}) \right]$$

$$= \frac{2 \times 1 \times 10^{-12}}{\beta_p \times 4.2} \left[\frac{0.06}{0.84} + 1.38 \right]$$

$$= \frac{0.69 \times 1 \times 10^{-12}}{\beta_p}$$

Thus, the rising time for both the 2-input NOR and NAND gates is:

$$t_r = \frac{0.69 \times 1 \times 10^{-12}}{40 \times 10^{-6} \times 7.2} = 2.4 \text{ ns}$$

(iii) Power in a cycle $= \frac{1}{2} C_L V_{DD}^2 f$

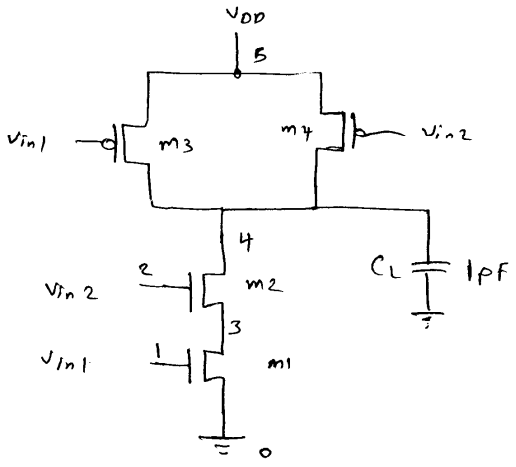
$$= \frac{1}{2} \times 1 \times 10^{-12} \times 25 \times f$$

$$= 12.5 \times 10^{-12} \times f \text{ W}$$

For example, if the frequency is 50 MHz

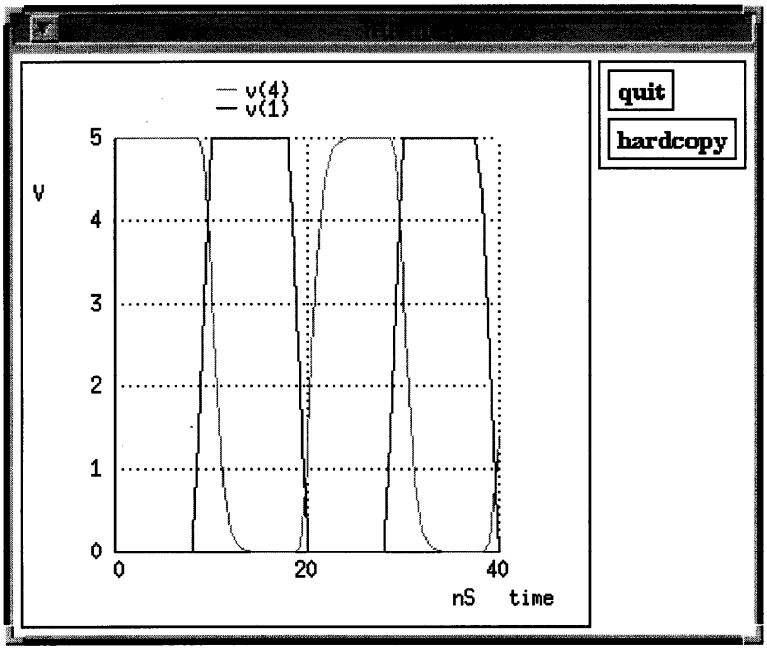
$\Rightarrow$ power $= 12.5 \times 10^{-12} \times 50 \times 10^{6} = 625 \mu W$.

(iv) NAND gate

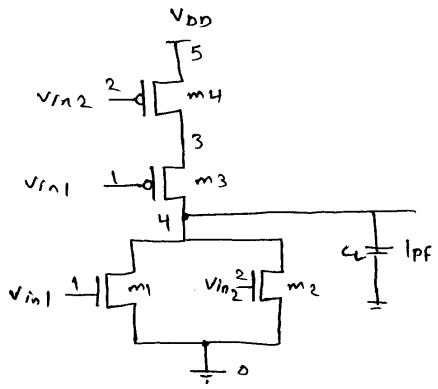



```
* NAND2 Circuit delay analysis
m1   3 1 0 0   nfet  w = 7.4u  L = 1u
m2   4 2 3 0   nfet  w = 7.4u  L = 1u
m3   4 1 5 5   pfet  w = 7.2u  L = 1u
m4   4 2 5 5   pfet  w = 7.2u  L = 1u
C1   4 0 1p
vdd  5 0 dc 5.0
vin1 1 0 dc pulse (0.0 5.0 8ns 2ns 2ns 8ns 20ns)
                                                )
vin2 2 0 dc 5.0
.model nfet nmos (vto = 1.0  kp = 100u)
.model pfet pmos (vto = -0.8  kp = 40u)
.tran 0.1ns 40ns
.print tran v(1) v(4)
.end
```

" NAND2 delay analysis "



NOR gate



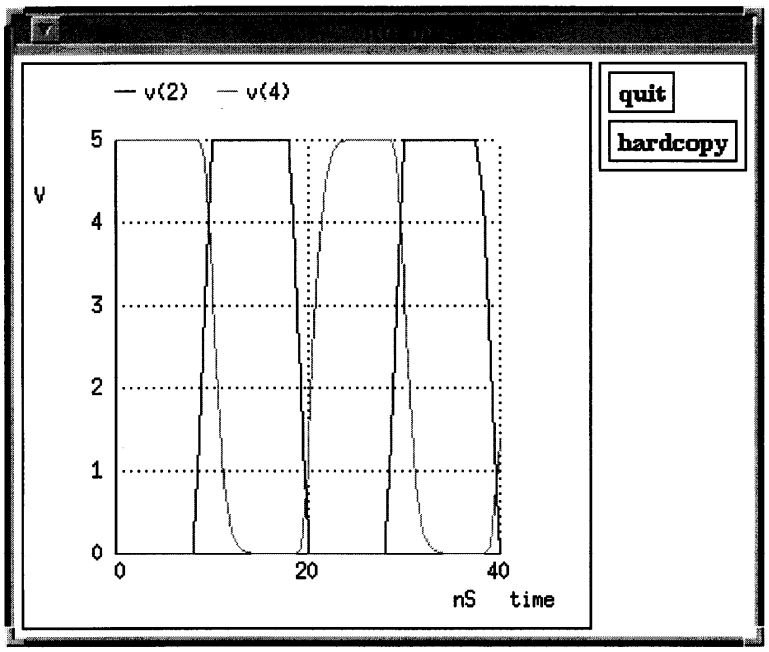

```
* NOR2 circuit delay analysis

m1    4  1  0  0   nfet   w=3.7u   L=1u
m2    4  2  0  0   nfet   w=3.7u   L=1M
m3    4  1  3  5   pfet   w=14.4u  L=1M
m4    3  2  5  5   pfet   w=14.4u  L=1M

C1    4  0  1p
vdd   5  0  dc  5.0
vin1  1  0  dc  0.0
vin2  2  0  dc  pulse (0.0 5.0 8ns 2ns 2ns 8ns 20ns)

.tran  0.1ns  40ns
.print tran v(2) v(4)
.model nfet nmos (vto = 1.0  Kp = 100u)
.model pfet pmos (vto = -0.8 Kp = 40u)
.end
```

"NOR2 Delay Analysis"



Note that this graph is identical to the NAND2 graph which is what we expected since we designed them to have identical rise and fall times.

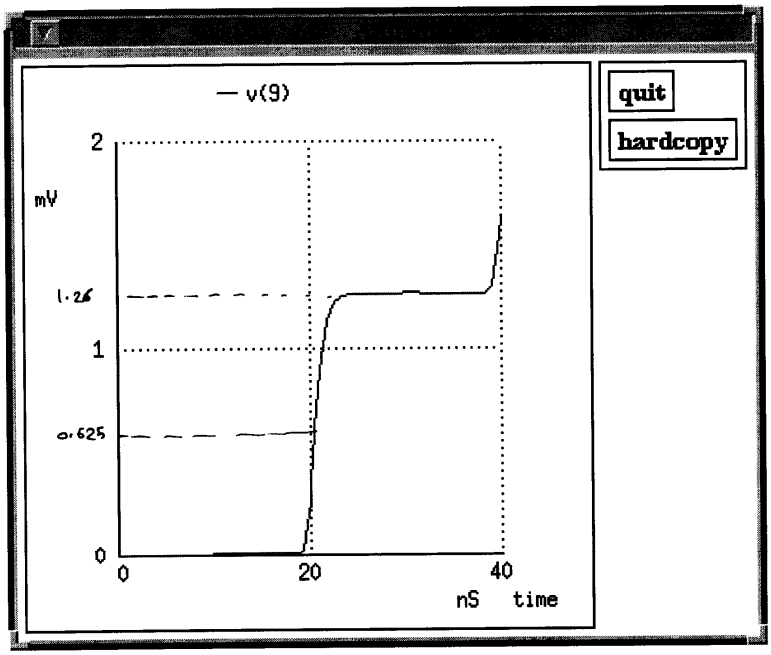
(v) Power meter

```
* NAND2 power meter simulation

m1   3  1  0  0   nfet  w = 7.4u  L=1u
m2   4  2  3  0   nfet  w = 7.4u  L=1u
m3   4  1  5  6   pfet  w = 7.2u  L=1u
m4   4  2  5  6   pfet  w = 7.2u  L=1u

C1   4  0  1p
Vdd  6  0  dc  5.0
Vstp 6  5  dc  0.0
fp   0  9  Vstp  0.025
rp   9  0  100K
cp   9  0  100p
Vin1 1  0  dc  pulse (0.0 5.0 8ns 2ns 2ns 8ns 20ns)
Vin2 2  0  dc  5.0
.model  nfet  nmos (Vto = 1.0  Kp =100u)
.model  pfet  pmos (Vto = -0.8  Kp =40u)
.tran   0.1ns  40ns
.print  tran  V(9)
.end
```

"NAND2 power meter simulation"



power = 0.625 mW

power due to both charging & discharging

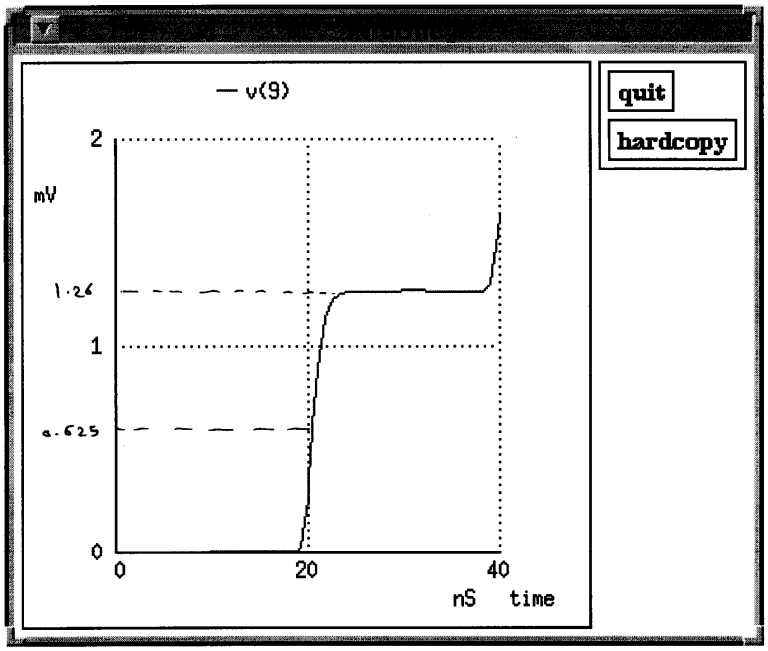
= 1.26 mV

```
* NOR2 power meter simulation

m1   4  1  0  0   nfet   w=3.7u   L=1u
m2   4  2  0  0   nfet   w=3.7u   L=1u
m3   4  1  3  6   pfet   w=14.4u  L=1u
m4   3  2  5  6   pfet   w=14.4u  L=1u

c1   4  0  1p
vdd  6  0  dc   5.0
vtstp 6 5  dc   0.0
fp   0  9  vtstp 0.025
rp   9  0  100K
cp   9  0  100p
vin1 1  0  dc  pulse (0.0 5.0 8ns 2ns 2ns 8ns 20ns)
vin2 2  0  dc  pulse (0.0 5.0 8ns 2ns 2ns 8ns 20ns)
.model nfet nmos ( vto = 1.0  kp = 100u)
.model pfet pmos ( vto = -0.8  kp = 40u)
.tran  0.1ns  40ns
.print tran v(9)
.end
```

"NOR2 power meter simulation"



* Note that it is also identical to the NAND2 power dissipated since power depend on the switching activity which is the same in this case.