

**COE 360, Principles of VLSI Design, Term 071**  
**HW# 6**

**Q.1.** Compute the gate, source, and drain capacitance for the NMOS transistor modeled in SPICE below. Assume that  $\epsilon_{\text{SiO}_2} = 3.9 \times 8.854 \times 10^{-14}$ , and that  $V_{\text{sb}} = 0$  and  $V_{\text{db}} = 2.5$  Volts.

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M1 4 3 5 0          NFET W=4U L=1U AS=15P AD=15P PS=10U PD=10U
.MODEL NFET NMOS
+ TOX=120E-8
+ CGBO=200P CGSO=600P CGDO=600P
+ CJ=200P CJSW=400P MJ=0.5 MJSW=0.3 PB=0.6
```

**Q.2.** A silicided word line is used for a RAM memory. Each memory cell has  $15 \mu\text{m}$  of  $1 \mu\text{m}$  metall,  $10 \mu\text{m}$  of  $1 \mu\text{m}$  poly (over field), and  $8 \mu\text{m}$  of  $1 \mu\text{m}$  gate capacitance. Assume that the gate capacitance is  $1800 \times 10^{-18} \text{ F}/\mu\text{m}^2$ , the poly-over-field oxide capacitance is  $50 \times 10^{-18} \text{ F}/\mu\text{m}^2$ , metall capacitance of  $30 \times 10^{-18} \text{ F}/\mu\text{m}^2$ , and silicide capacitance of  $20 \times 10^{-18} \text{ F}/\mu\text{m}^2$ .

- (i) Calculate the per-cell load and the load for 32 memory cells in a row.
- (ii) What would be the word-line RC delay from a buffer using 2mm long silicide,  $1 \mu\text{m}$  wide ( $4\Omega SQ$ ).
- (iii) How wide would the word line have to be to keep the delay below 2ns.

**Q.3.** Consider a 2-input CMOS NOR gate. The characteristics of its nMOS transistors are specified as follows: When  $V_{\text{GS}} = 5\text{V}$ , the drain current for each nMOS transistor reaches its saturation level  $I_{\text{sat}} = 2 \text{ mA}$  for  $V_{\text{DS}} > 4.0\text{V}$ , assuming  $(W/L)_n = 2$ . Assume that both inputs receive a step pulse that switches instantaneously from 0V to 5V. Using the data above, calculate the delay time necessary for the output to fall from its initial value of 5V to 2.5 V, assuming an output load capacitance of  $1.0 \text{ pF}$ . What will be the delay if  $(W/L)_n = 4$ .

**Q.4.** A CMOS fabrication process has the following parameters:

$\mu_n C_{\text{ox}} = 100 \text{ uA}/\text{V}^2$ ,  $\mu_p C_{\text{ox}} = 40 \text{ uA}/\text{V}^2$ ,  
 $L = 1 \mu\text{m}$  for both nMOS and pMOS devices.  
 $V_{\text{tn}} = 1.0 \text{ V}$ ,  $V_{\text{tp}} = -0.8 \text{ V}$ .

- (i) Design both a 2-input CMOS NOR gate and a 2-input CMOS NAND gate such that  $V_{\text{th}} = 2.5\text{V}$  for  $V_{\text{DD}} = 5\text{V}$ , and falling time of 2ns with a load capacitance of  $1 \text{ pF}$  and ideal step inputs.
- (ii) Calculate the rising time for both gates.
- (iii) Determine the maximum power dissipated in a cycle for both gates.
- (iv) Simulate both gates using SPICE and compare the measured rising and falling times to specifications.
- (v) Use the power-meter method to measure the maximum power dissipation in a cycle for both gates, and compare the results to your calculation.