HW#5

Q1 Average DC power dissipation $= \frac{V_{DD}}{2}\frac{(V_{DD}-V_{OL})}{R_L}$

$\Rightarrow 100\,\mu W = \frac{5}{2}\frac{(5-V_{OL})}{120\,K\Omega} \Rightarrow V_{OL} = 0.2\,V$

When $V_{out} = V_{OL}$, $V_{in} = V_{OH} = V_{DD}$

$V_{gd} = V_{DD} - V_{OL} > V_t \Rightarrow$ transistor is linear

By KCL: $\frac{V_{DD}-V_{OL}}{R_L} = \frac{\beta}{2}\left[2(V_{DD}-V_t)V_{OL} - V_{OL}^2\right]$

$\Rightarrow \beta R_L = \frac{2(V_{DD}-V_{OL})}{\left[2(V_{DD}-V_t)V_{OL} - V_{OL}^2\right]}$

$= \frac{2(5-0.2)}{\left[2(5-0.8)0.2 - (0.2)^2\right]}$

$= \frac{9.6}{[1.68-0.04]} = 5.854$

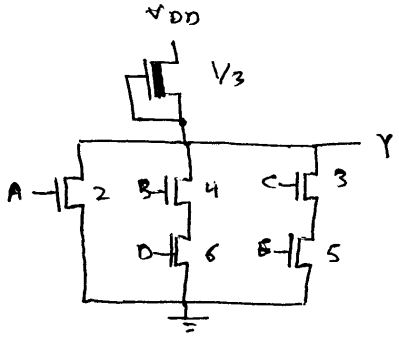
For a resistive-load inverter,

$V_{IL} = V_t + \frac{1}{R_L\beta} = 0.8 + \frac{1}{5.854} = 0.971\,V$

and $V_{out}(V_{IL}) = V_{DD} - \frac{1}{2R_L\beta} = 5 - \frac{1}{2(5.854)}$

$= 4.91\,V$

Q2 (i)



For a depletion-load inverter,

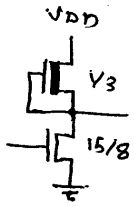
$$V_{OL} = V_{OH} - V_{T_0} - \sqrt{(V_{OH} - V_{T_0})^2 - \frac{\beta_{load}}{\beta_{driver}} |V_{T,load}(V_{OL})|^2}$$

The worst or highest V_{OL} is obtained when C = H and E = H, while all other inputs are low. This is because this combination produces the highest pull-down resistance or the smallest equivalent β_{driver}. This in turn produces the highest V_{OL}.

Let us first find the inverter-equivalent circuit for this combination.

$$\left(\frac{W}{L}\right)_{equiv} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_C} + \frac{1}{\left(\frac{W}{L}\right)_E}} = \frac{1}{\frac{1}{3} + \frac{1}{5}} = \frac{1}{\frac{8}{15}} = \frac{15}{8}$$

$$\frac{\beta_{load}}{\beta_{driver}} = \frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_{load}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_{driver}} = \frac{V3}{15/8} = \frac{8}{45} = 0.18$$



To compute V_{OL}, we first assume

$V_{T,load}(V_{OL}) = -2.5$

$$\Rightarrow V_{OL} = 5 - 1 - \sqrt{(5-1)^2 - \frac{8}{45}(2.5)^2} = 0.14\ V$$

Next, we compute the value of $V_{T,load}$ as a function of V_{OL}.

$$V_{T,load}(V_{OL}=0.14) = V_{T0,load} + \gamma\left[\sqrt{2\phi_b + V_{OL}} - \sqrt{2\phi_b}\right]$$
$$= -2.5 + 0.4\left[\sqrt{0.6+0.14} - \sqrt{0.6}\right]$$
$$= -2.147\ V$$

Then, we recompute V_{OL} with the updated value of $V_{T,load}$

$$V_{OL} = 4 - \sqrt{16 - \frac{8}{45}(2.147)^2} \approx \underline{0.14}\ V$$

So, we stop here.

The best or lowest V_{OL} is achieved when all inputs are high. This combination produces the lowest pull-down resistance or the largest equivalent β_{driver}. First, let us find the inverter equivalent circuit for this combination.

$$\left(\frac{W}{L}\right)_{equiv} = \left(\frac{W}{L}\right)_A + \frac{1}{\frac{1}{(\frac{W}{L})_B} + \frac{1}{(\frac{W}{L})_D}} + \frac{1}{\frac{1}{(\frac{W}{L})_C} + \frac{1}{(\frac{W}{L})_E}}$$
$$= 2 + \frac{1}{\frac{1}{4}+\frac{1}{6}} + \frac{1}{\frac{1}{3}+\frac{1}{5}}$$
$$= 2 + \frac{24}{10} + \frac{15}{8} = 6.275$$

$$\frac{\beta_{load}}{\beta_{driver}} = \frac{V_3}{6.275} = 0.053$$

Since V_{OL} will be very small, we can assume that the body bias effect is negligible.

$$V_{OL} = 4 - \sqrt{16 - 0.05(2.5)^2} = \underline{0.04}\ V$$

(ii) We need to design the circuit to achieve a worst case $V_{OL} = 0.1\,V$.

Since the output value is small, we can neglect the body-bias effect.

$$0.1 = 4 - \sqrt{16 - \frac{\beta_{load}}{\beta_{driver}}(2.5)^2}$$

$$\Rightarrow 3.9 = \sqrt{16 - \frac{\beta_{load}}{\beta_{driver}}(2.5)^2}$$

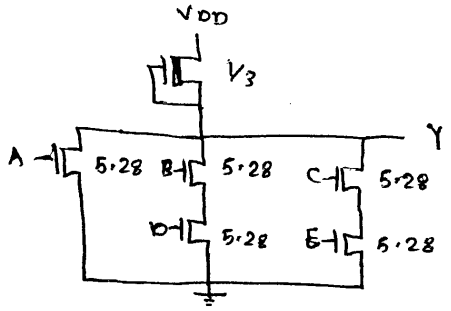
$$\Rightarrow 15.21 = 16 - \frac{\beta_{load}}{\beta_{driver}}(6.25) \Rightarrow \frac{\beta_{load}}{\beta_{driver}} = 0.126$$

Thus, $\left(\frac{W}{L}\right)_{driver} = \left(\frac{W}{L}\right)_{load} \times \frac{1}{0.126} = 2.64$

If we assume that all $\frac{W}{L}$ for all the nmos transistors are equivalent, then the worst case is when two transistors in series are on

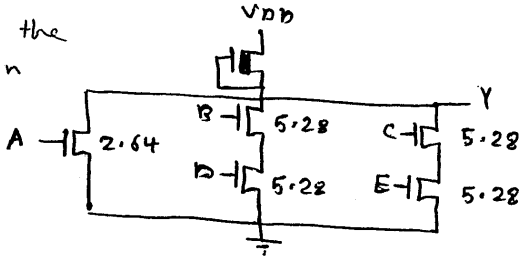
$$\Rightarrow \left(\frac{W}{L}\right)_{equiv} = \frac{1}{2}\left(\frac{W}{L}\right) \Rightarrow \left(\frac{W}{L}\right) = 2\left(\frac{W}{L}\right)_{equiv}$$

$$= 2 \times 2.64 = 5.28$$

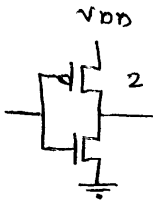


or we can have the following design, which achives the same V_{OL} for all single paths from output to ground.

* Note that the second design has less area.



Q3 CMOS Inverter



(i) $V_{th} = 2.5\ V$, $V_{DD} = 5V$

Since $V_{th} = \frac{V_{DD}}{2}$ and

$V_{tn} = |V_{tp}| \Rightarrow \frac{\beta_n}{\beta_p} = 1$

$$\Rightarrow \frac{\mu_n C_{ox} \left(\frac{W}{L}\right)_n}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p} = 1$$

$$\Rightarrow \left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n \times \frac{\mu_n C_{ox}}{\mu_p C_{ox}} = \left(\frac{W}{L}\right)_n \times \frac{100}{40}$$

$$= 2.5 \left(\frac{W}{L}\right)_n$$

$$\Rightarrow \left(\frac{W}{L}\right)_n = 0.4 \left(\frac{W}{L}\right)_p$$

since $\left(\frac{W}{L}\right)_p$ is given as 2 $\Rightarrow \left(\frac{W}{L}\right)_n = 0.8$

(ii) For a symmetric inverter, $NM_H = NM_L = V_{IL}$

$$V_{IL} = \frac{1}{8}(3 V_{DD} + 2 V_{tn})$$

$$= \frac{1}{8}(15 + 2) = 2.125\ V$$

Thus, $NM_H = NM_L = 2.125\ V$

Q4

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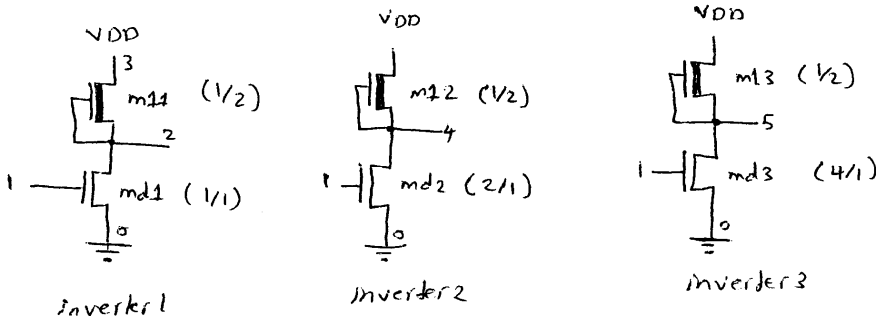
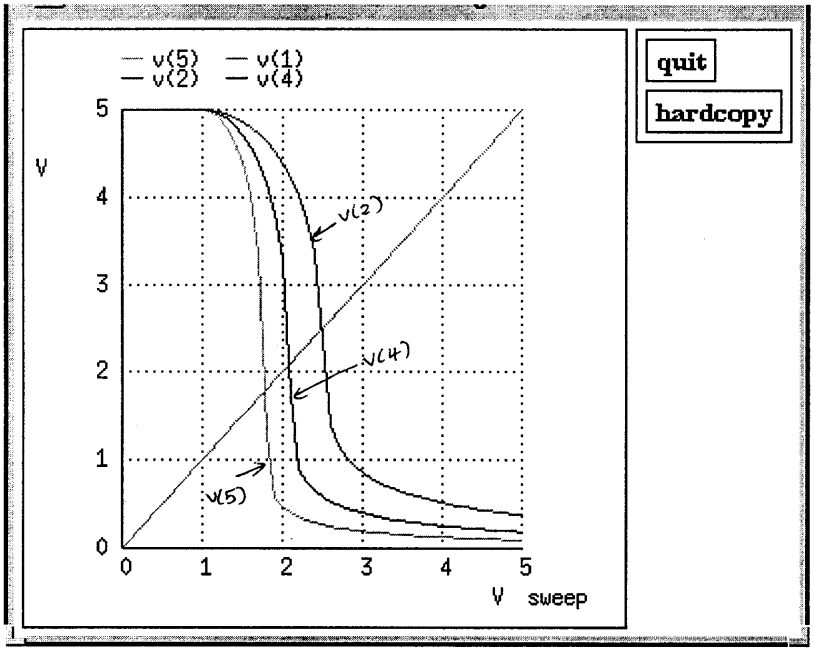
* Depletion-Load Inverter Circuit
VDD 3 0 DC 5
md1 2 1 0 0 emode W=1u L=1u
ml1 3 2 2 0 dmode W=1u L=2u
md2 4 1 0 0 emode W=2u L=1u
ml2 3 4 4 0 dmode W=1u L=2u
md3 5 1 0 0 emode W=4u L=1u
ml3 3 5 5 0 dmode W=1u L=2u
VS 1 0 DC
.model emode nmos (vto=1.0 gamma=0.4 phi=0.6 kp=100u)
.model dmode nmos (vto=-2.5 gamma=0.4 phi=0.6 kp=100u)
.DC VS 0 5 0.1
.print dc v(2) v(4) v(5)
.end
```



Inverter		$\beta_{driven} / \beta_{load}$
1	v(2)	2
2	v(4)	4
3	v(5)	8

we can observe from the voltage transfer characteristic graphs that for a depletion-load inverter, it is necessary to have a large $\beta_{driver}/\beta_{load}$ ratio. The larger this ratio is the lower the value of V_{OL}. Note also that this reduces the values of V_{IL}, V_{IH} and V_{th}. NM_H will increase but NM_L might be the same.



Q5

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* CMOS Inverter Circuit
VDD 3 0 DC 5
md1 2 1 0 0 MN W=1u L=1u
ml1 2 1 3 3 MP W=2u L=1u
md2 4 1 0 0 MN W=2u L=1u
ml2 4 1 3 3 MP W=2u L=1u
md3 5 1 0 0 MN W=4u L=1u
ml3 5 1 3 3 MP W=2u L=1u
VS 1 0 DC
.model MN nmos (vto=1.0 gamma=0.4 phi=0.6 kp=100u)
.model MP pmos (vto=-1.0 gamma=0.4 phi=0.6 kp=40u)
.DC VS 0 5 0.1
.print dc v(2) v(4) v(5), I(vdd)
.end
```
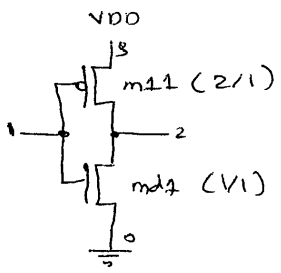
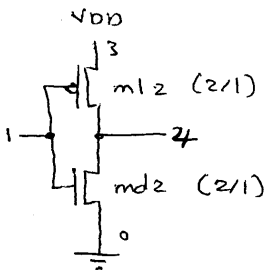
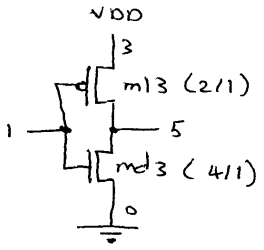



inverter 1



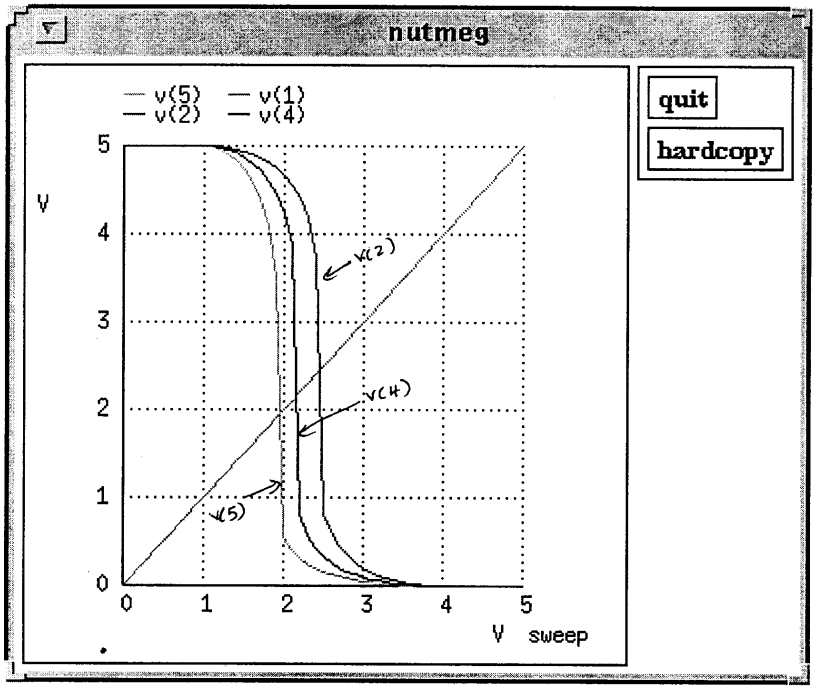
inverter 2



inverter 3

Inverter		β_n / β_p
1	v(2)	1.25
2	v(4)	2.5
3	v(5)	5

A Key parameter in the design of CMOS inverters is the inverter threshold voltage. All CMOS inverters have a $V_{OL}=0$ and $V_{OH}=V_{DD}$. We can see here that as β_n/β_p is close to 1, V_{th} is close to $V_{DD}/2$ since $V_{tn}=|V_{tp}|$. The larger the ratio of $\frac{\beta_n}{\beta_p}$, the smaller the value of V_{th}. In CMOS inverters, we can be close to the behavior of an ideal inverter using a small $(W/L)_n/(W/L)_p$ ratio, nearly equal to $\sqrt{2.5}$ for a symmetric inverter, i.e. $(\frac{W}{L})_p \simeq 2.5\,(\frac{W}{L})_n$.



For nmos inverters, larger ratio $\beta_{driver}/\beta_{load}$ is required which implies $(\frac{W}{L})_{driver}$ has to be larger than $(\frac{W}{L})_{load}$.

Q6 (i) For the first shape:

$$R = 1\,R_s + 0.66\,R_s + 0.66\,R_s + 4\,R_s + 0.66\,R_s + 0.66\,R_s + 1\,R_s$$

$$= 8.64\,R_s$$

Material	Resistance	
Polysilicon	$8.64 \times 20 =$	172.8 Ω
n-diffusion	$8.64 \times 40 =$	345.6 Ω
p-diffusion	$8.64 \times 150 =$	1296 Ω
metal	$8.64 \times 0.05 =$	0.432 Ω

For the second shape:

$$R = 1\,R_s + \frac{2}{3}\,R_s + \frac{1.5}{5}\,R_s + \frac{2.5}{2}\,R_s$$

$= 3.22\,R_s$ (Note that for simplicity, corners are ignored).

Material	Resistance	
Polysilicon	$3.22 \times 20 =$	64.4 Ω
n-diffusion	$3.22 \times 40 =$	128.8 Ω
p-diffusion	$3.22 \times 150 =$	483 Ω
metal	$3.22 \times 0.05 =$	0.161 Ω

(ii) * The channel resistance of the p-transistor equals the resistance of two resistors in series R_1 and R_2. R_1 equals to $\frac{3}{2} R_s$. R_2 is a parallel combination of three resistors, two of which have nonuniform current flow.

$$\frac{1}{R_2} = \frac{1}{1 R_s} + \frac{1}{2(0.66) R_s} + \frac{1}{2(0.66) R_s}$$

$$\frac{1}{R_2} = \frac{1 + 0.76 + 0.76}{R_s} = \frac{2.52}{R_s}$$

$$\Rightarrow R_2 = 0.398\ R_s$$

$$\Rightarrow R_p = R_1 + R_2 = 1.5\ R_s + 0.398\ R_s$$

$$= 1.898\ R_s$$

$$= 1.898 \times 15 \times 10^3$$

$$= \underline{\underline{28.47\ K\Omega}}$$

* The channel resistance of the n-transistor consists of three resistances in parallel.

$$\frac{1}{R_n} = \frac{1}{\frac{1}{4} R_s} + \frac{1}{(0.66) R_s} + \frac{1}{\frac{1}{2} R_s}$$

$$= \frac{4 + 1.52 + 2}{R_s} = \frac{7.52}{R_s}$$

$$\Rightarrow R_n = \frac{1}{7.52} R_s = \frac{1}{7.52} \times 6 \times 10^3$$

$$= \underline{\underline{0.798\ K\Omega}}$$