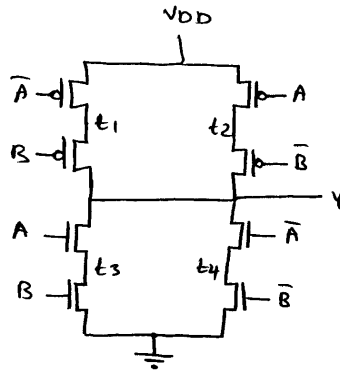
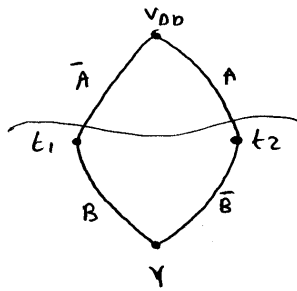


HW#4

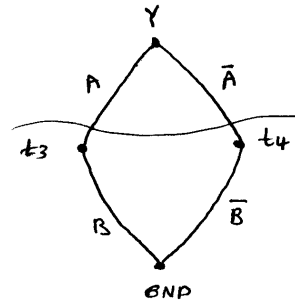
Q1 (i)



p-network

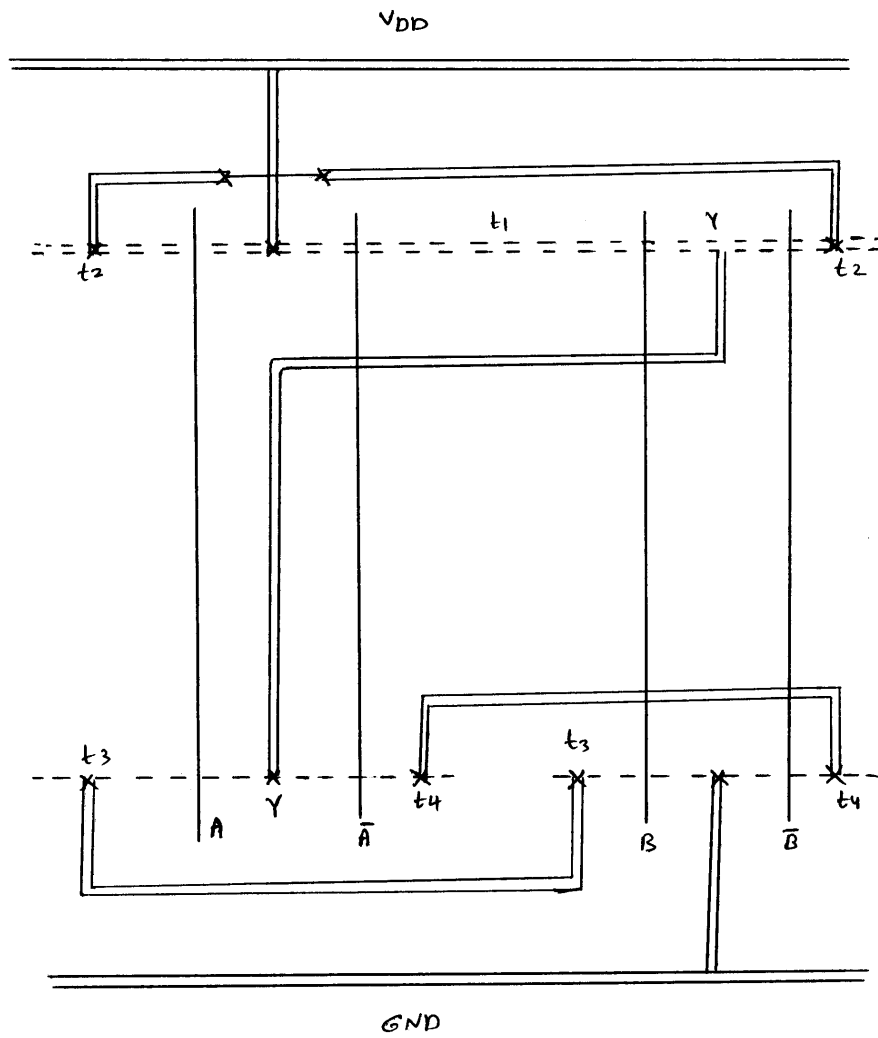


n-network

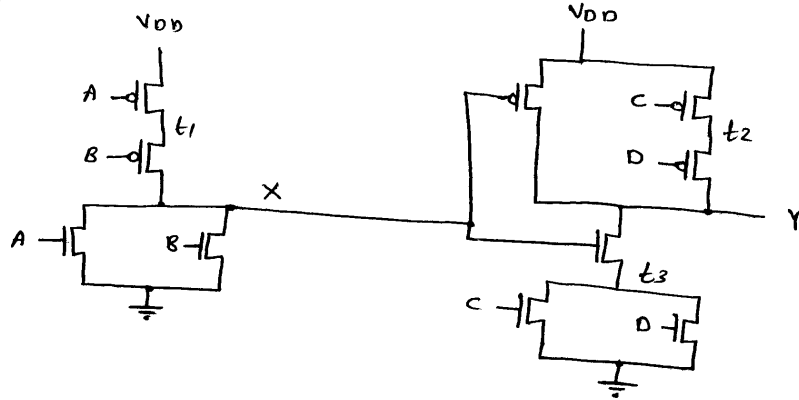


Since we can't find a common Euler path, we partition the graphs into two subgraphs such that a common Euler path is found. one way of partitioning the networks is shown above where we have the two Euler paths $\{A, \bar{A}\}$, $\{B, \bar{B}\}$

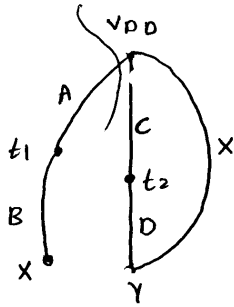
Stick Diagram Layout :



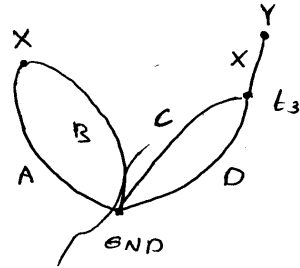
(ii)



p-network

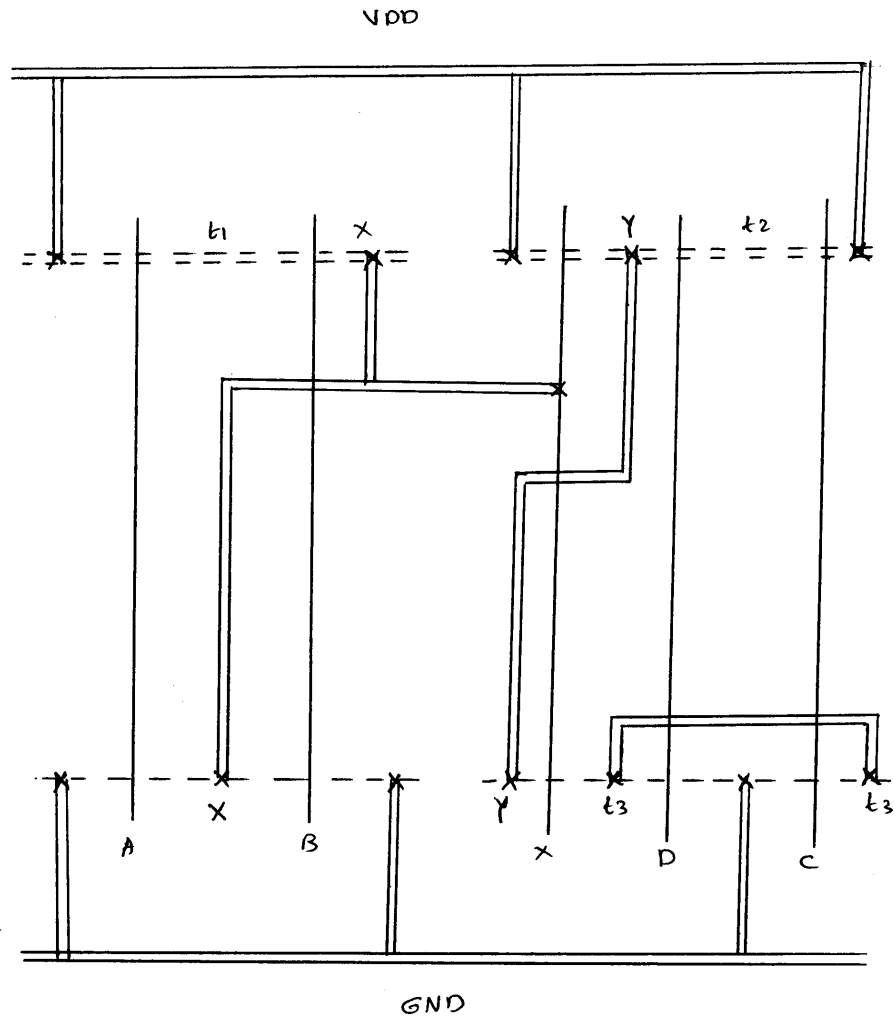


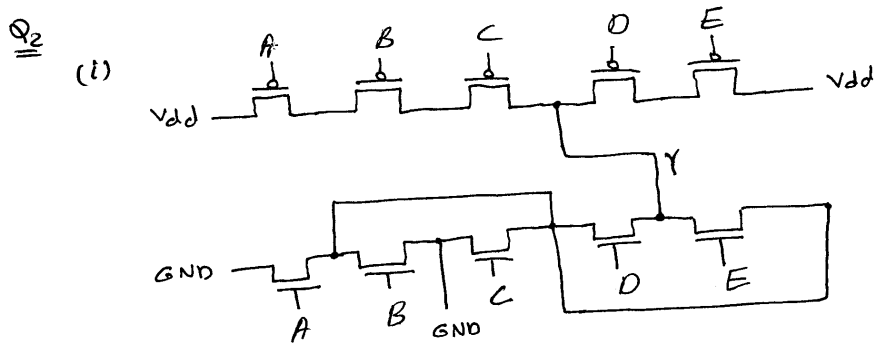
n-network



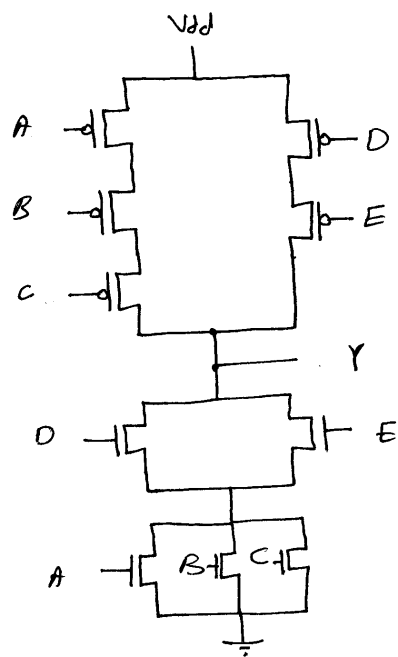
we can't find a common Euler path, so we partition the graphs into two subgraphs as shown above, Note that there several choices possible. Then, we have the two Euler paths $\{A, B\}$ and $\{X, D, C\}$

Stick Diagram Layout :



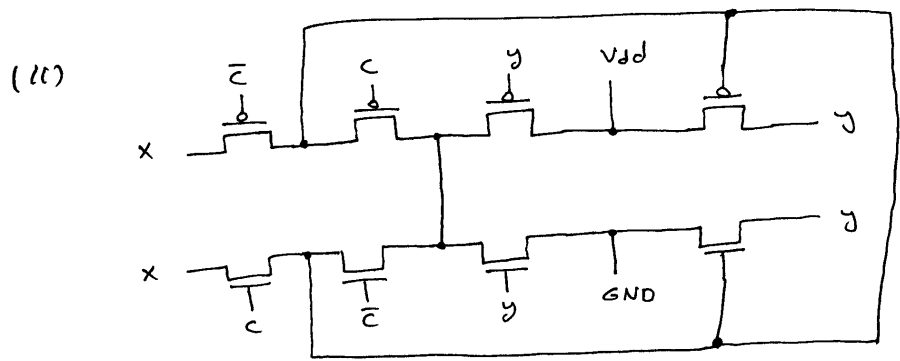


We can rearrange this as follows:

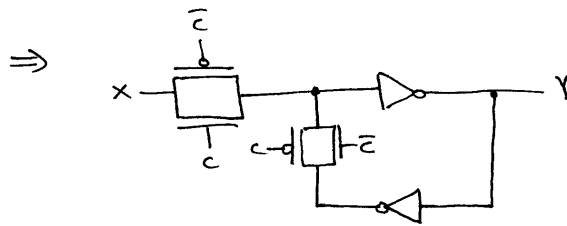
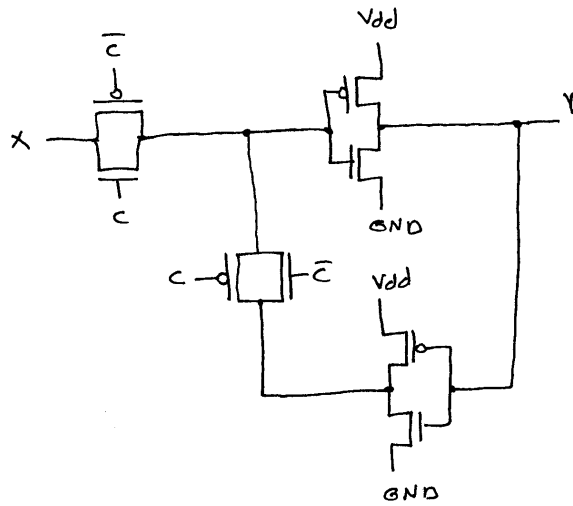


$$\text{So, } Y = [(D+E)(A+B+C)]'$$

$$\text{or } Y = \bar{A}\bar{B}\bar{C} + \bar{D}\bar{E}$$

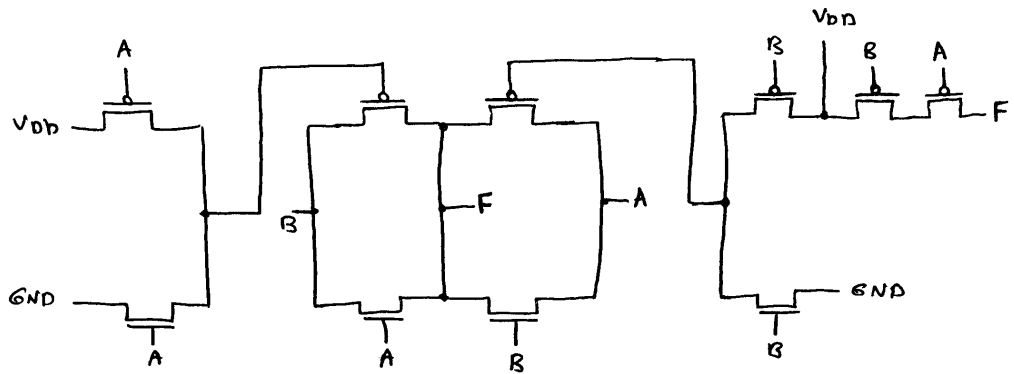


We can rearrange this as follows:

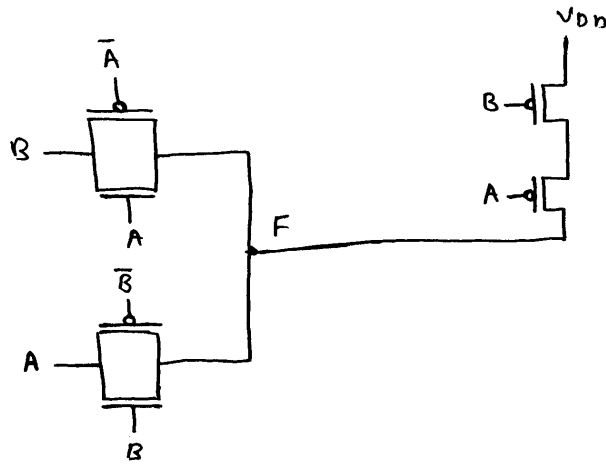


We can see that this implements a D-latch where x is the D input, and c the clock input. Y here is \bar{Q} .

Q3



We can rearrange this as follows:



A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

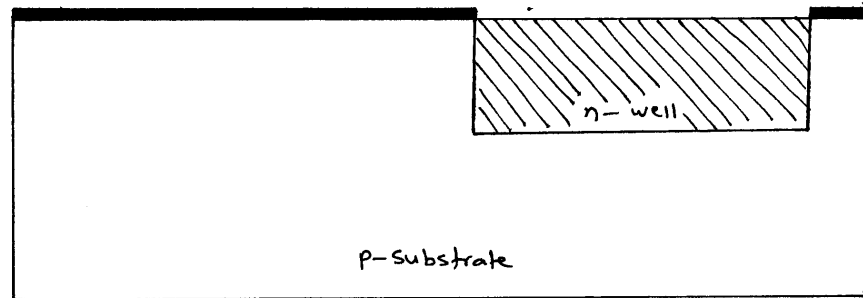
$$F = \bar{A}\bar{B} + AB$$

$$= A \text{ XNOR } B$$

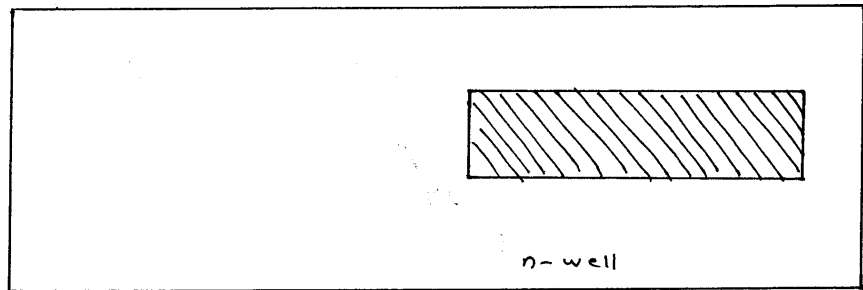
Q.4

(a) n-well mask

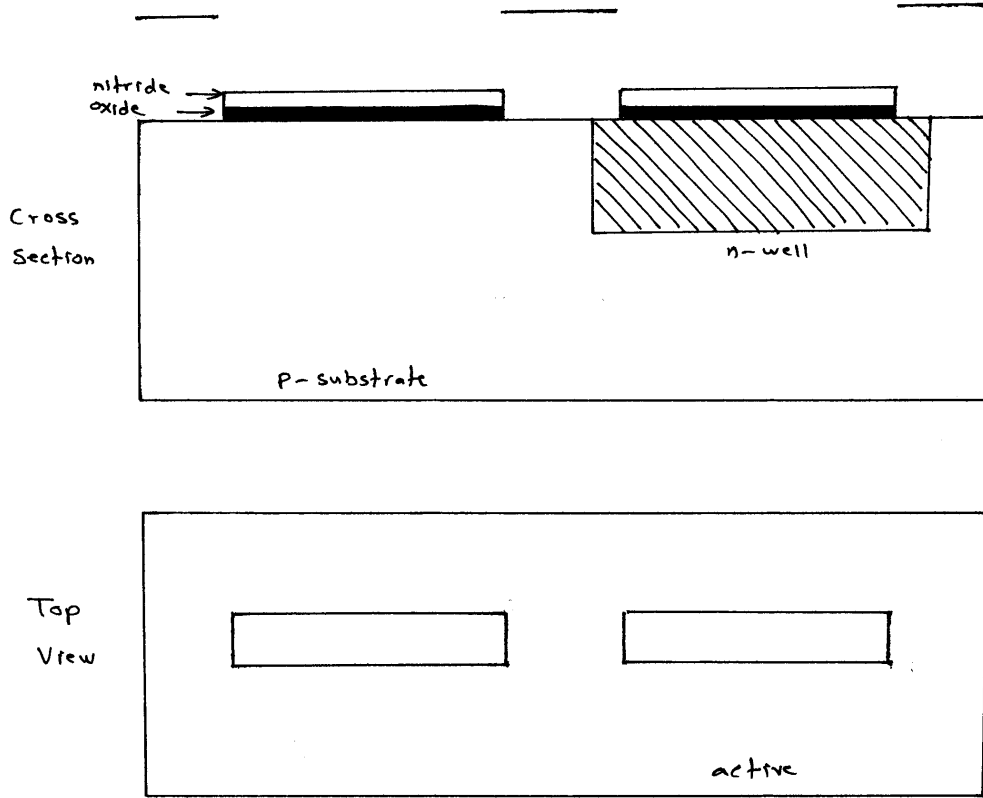
Cross
Section



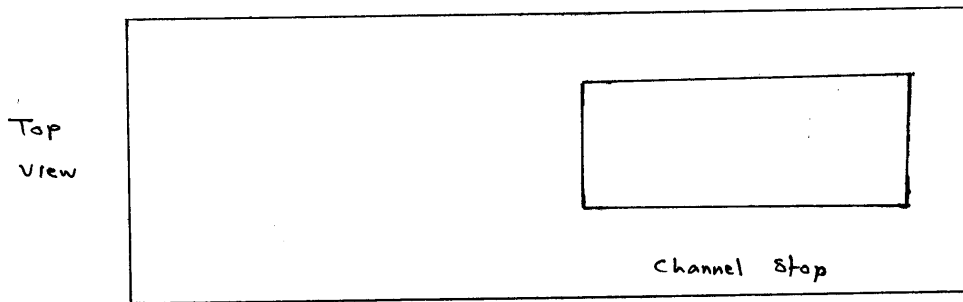
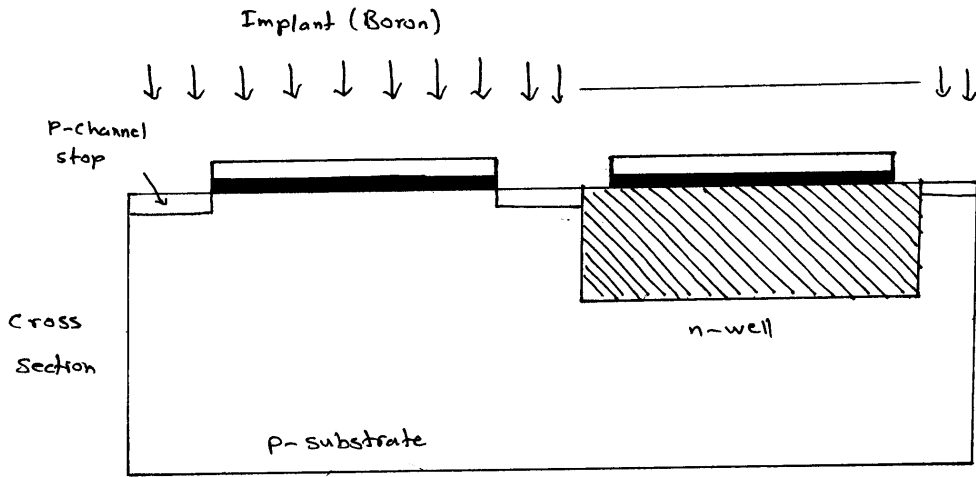
Top
View



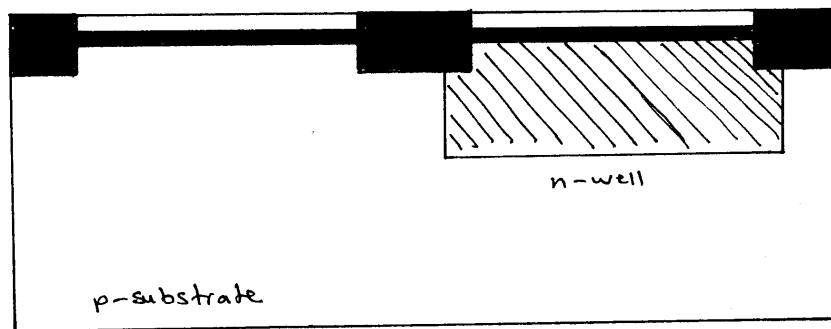
(b) Active mask



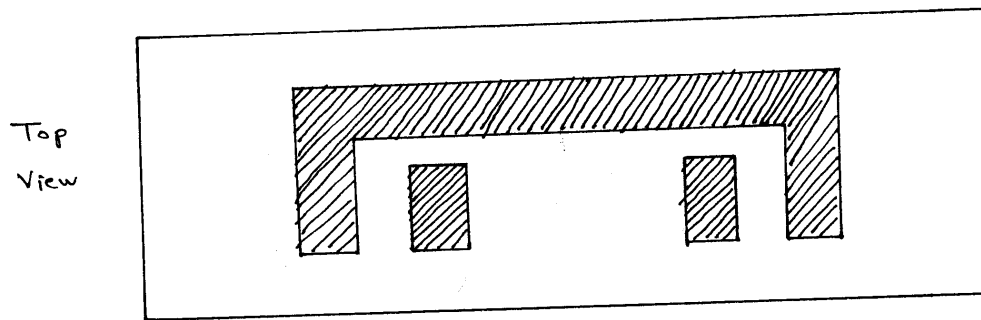
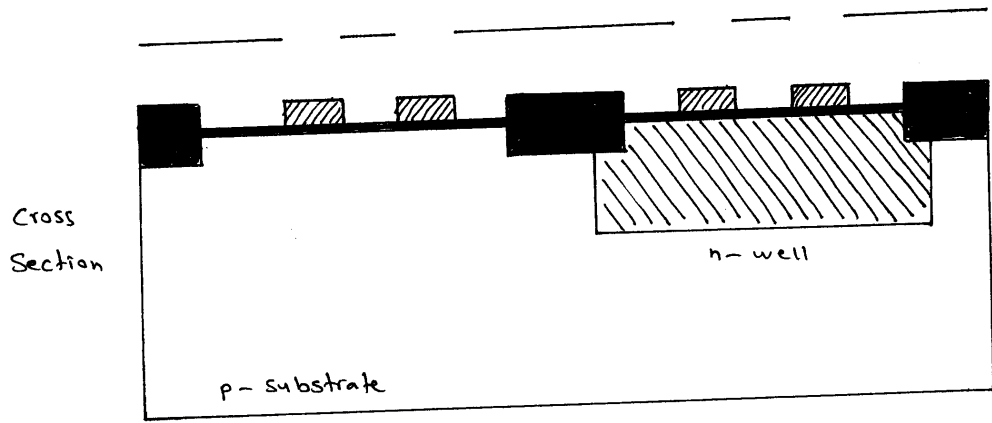
(c) channel stop mask:



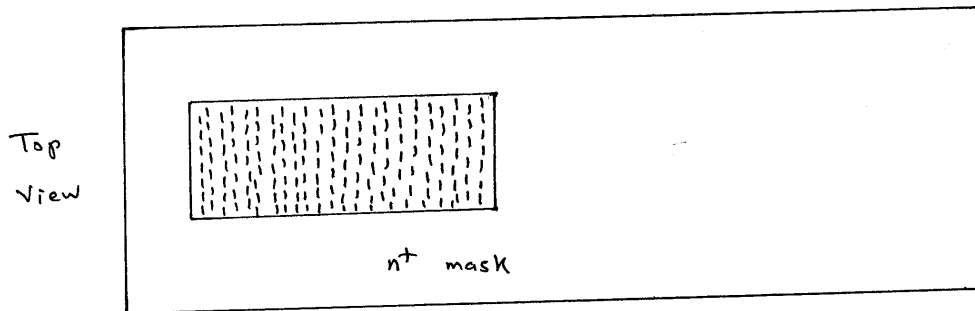
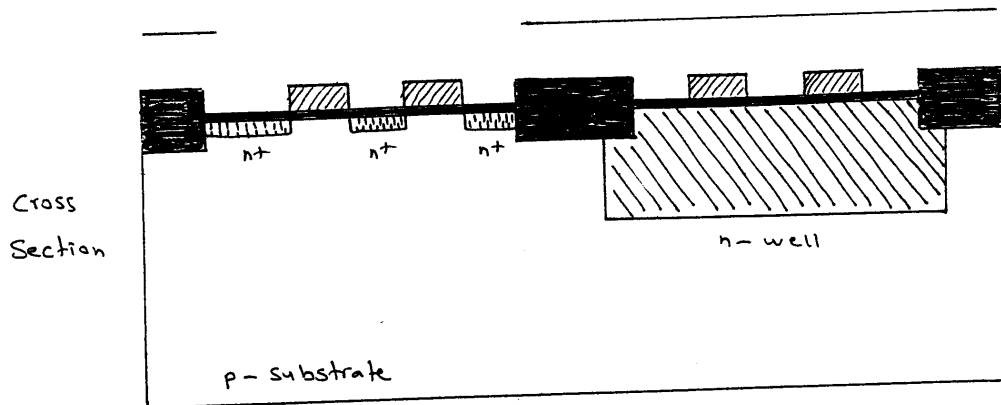
(d) Field Oxide Growth



(e) polysilicon mask

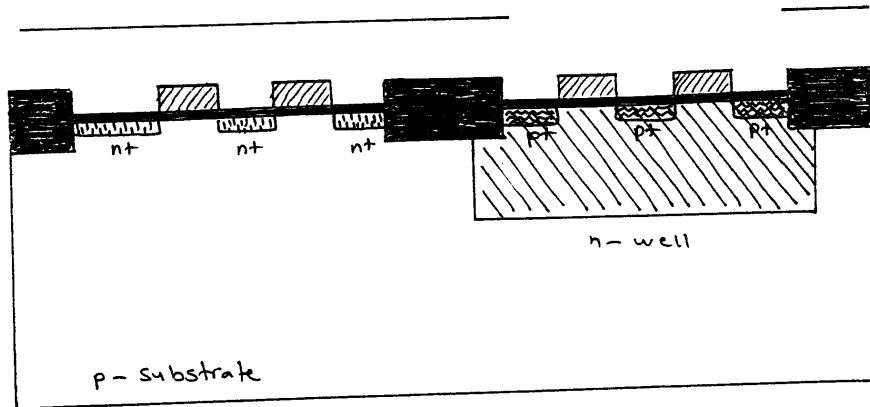


(f) n^+ mask

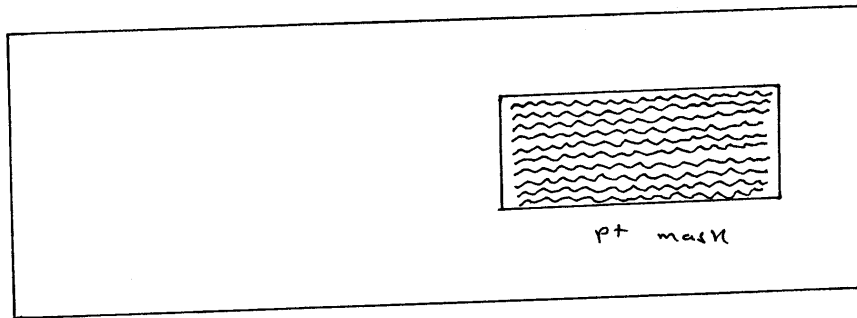


(9) pt mask

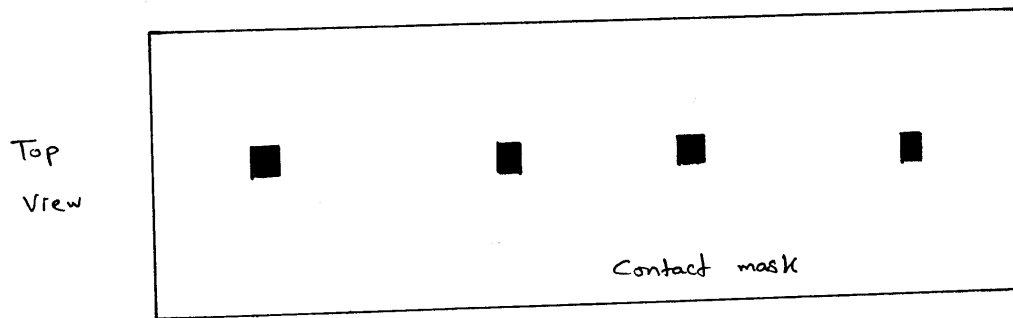
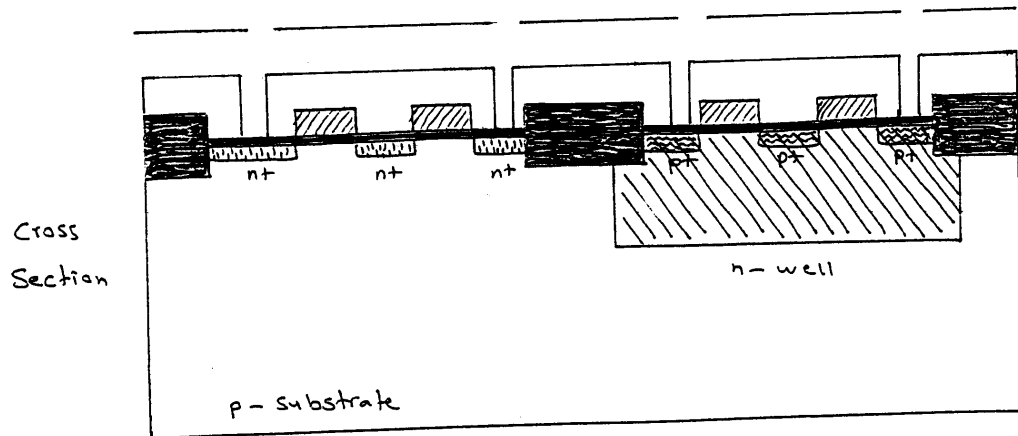
Cross
Section



Top
View



(h) Contact Mask



(c) Metal Mask

Cross
Section

