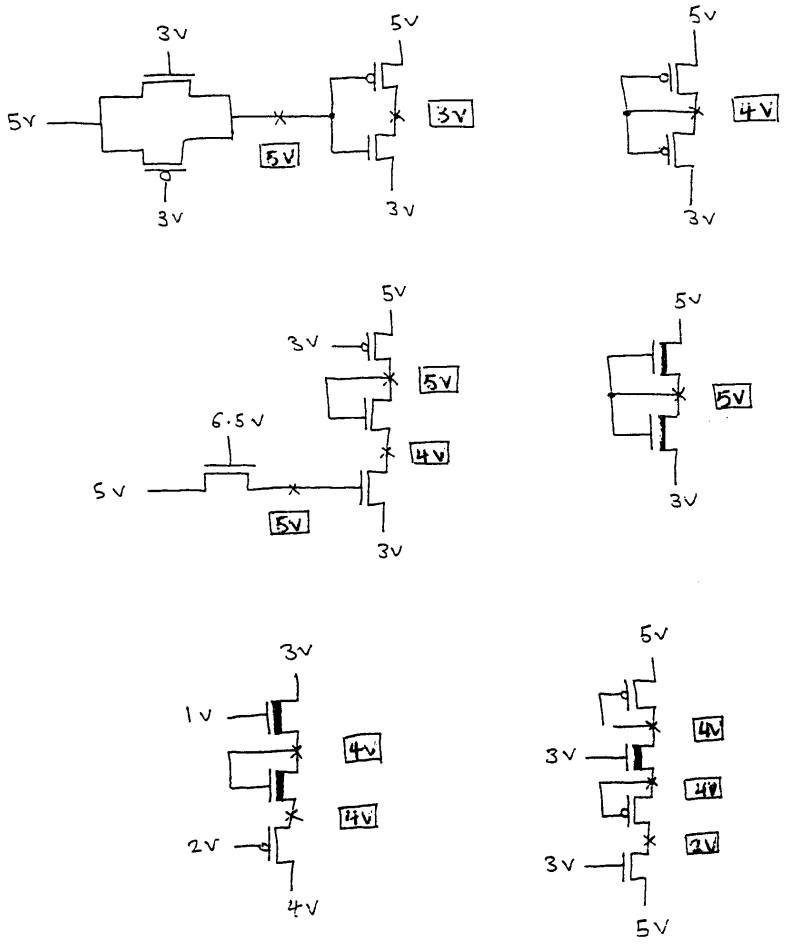
COE 360

Dr. Aiman El-Maleh

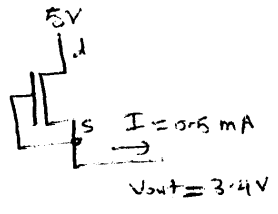
HW#3

Q.1. Assuming nMOS enhancement transistor threshold voltage V_{tn} of 1.0 V, depletion transistor threshold voltage V_{td} of -2.0 V, and pMOS enhancement transistor threshold voltage V_{tp} of -1.0 V, write down the voltages of the indicated nodes below. Assume that the body effect is negligible.



Q2 (i) Depletion-type nmos transistor

$\mu C_{ox} = 200\ \mu A/V^2$, $V_{td} = -2\ V$, $\gamma = 0.5V$, $2\phi_b = 0.6V$



$V_{sb} \neq 0 \Rightarrow$ there is body bias

$$V_t = V_{to} + \gamma\left[\sqrt{2\phi_b + |V_{sb}|} - \sqrt{2\phi_b}\right]$$

$$= -2 + \frac{1}{2}\left[\sqrt{0.6 + 3.4} - \sqrt{0.6}\right]$$

$$= -1.387\ V$$

$V_{gs} = 0 > -1.38V$, $V_{gd} = -1.6 < -1.387\ V$

$\Rightarrow$ transistor will be in saturation when

$V_{out} = 3.4V$

$$I_D = \frac{\beta}{2}\left[V_{gs} - V_t\right]^2$$

$$\Rightarrow \beta = \frac{2 I_D}{\left[V_{gs} - V_t\right]^2} = \frac{2 \times 0.5 \times 10^3\ \mu A}{\left[0 + 1.387\right]^2}$$

$$= 519.59\ \frac{\mu A}{V^2}$$

$$\beta = \mu C_{ox}\frac{W}{L} \Rightarrow \frac{W}{L} = \frac{\beta}{\mu C_{ox}} = \frac{519.59}{200}$$

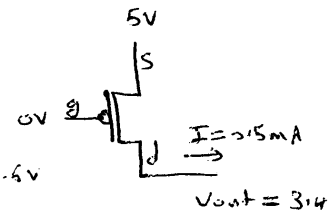
$$= 2.598$$

Since $L = 1\mu \Rightarrow W = 2.598\ \mu$

However, since the minimum grid size is

$0.25 \Rightarrow W = 2.75\ \mu$

(ii) PMOS transistor



$V_{sb} = 0 \Rightarrow$ No bias effect

$V_{tp} = -1\ V$

$\mu C_{ox} = 40\ \mu A/V^2$, $\gamma = 0.5\ V^{1/2}$, $2\phi_b = 0.6\ V$

$V_{gs} = -5\ V < -1\ V$, $V_{ds} = -1.6\ V$

$V_{gd} = -3.4\ V < -1 \Rightarrow$ transistor will be linear when $V_{out} = 3.4$

$$I_D = \frac{\beta}{2}\left[2(V_{gs} - V_t)V_{ds} - V_{ds}^2\right]$$

$$\Rightarrow \beta = \frac{2 I_D}{\left[2(V_{gs} - V_t)V_{ds} - V_{ds}^2\right]}$$

$$= \frac{2 \times 0.5 \times 10^3\ \mu A}{\left[2(-5+1)(-1.6) - (-1.6)^2\right]}$$

$$= 97.66\ \frac{\mu A}{V^2}$$

$$\frac{W}{L} = \frac{\beta}{\mu C_{ox}} = \frac{97.66}{40} = 2.44$$

Since $L = 1\mu \Rightarrow W = 2.44\ \mu$

However, since the minimum grid size is 0.25

$\Rightarrow W = 2.5\ \mu$

Q3

1. $V_{gs} = V_{ds} = 9\,V \Rightarrow V_{gd} = 0 < V_{tn}$

$\Rightarrow$ transistor is in saturation

$$I_D = \frac{\beta}{2}\left[V_{gs} - V_t\right]^2$$

$$\Rightarrow 2\,mA = \frac{\beta}{2}\left[9 - V_t\right]^2 \Rightarrow \beta = \frac{4\,mA}{[9 - V_t]^2}$$

2. $V_{gs} = V_{ds} = 5V \Rightarrow V_{gd} = 0 < V_{tn}$

$\Rightarrow$ transistor is in saturation

$$\Rightarrow 0.5\,mA = \frac{\beta}{2}\left[5 - V_t\right]^2 \Rightarrow \beta = \frac{1\,mA}{[5 - V_t]^2}$$

Equating the equations in (1) & (2)

$$\Rightarrow \frac{4\,mA}{[9 - V_t]^2} = \frac{1\,mA}{[5 - V_t]^2}$$

$$\Rightarrow \frac{2}{9 - V_t} = \frac{1}{5 - V_t}$$

$$\Rightarrow 9 - V_t = 10 - 2V_t \Rightarrow \boxed{V_t = 1V}$$

Thus, $\beta = \frac{1\,mA}{[5 - V_t]^2} = \frac{1\,mA}{16} = \underline{\underline{62.5\,\frac{\mu A}{V^2}}}$