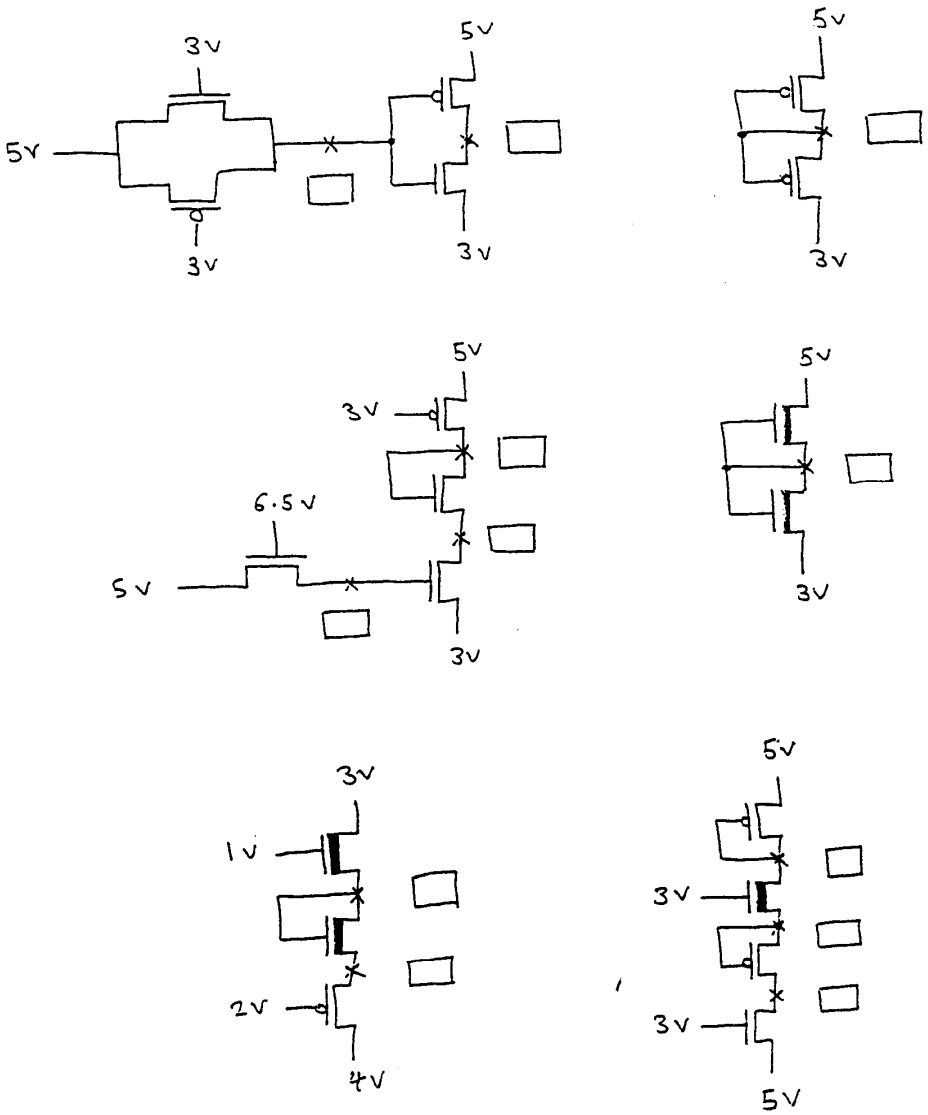
COE 360, Principles of VLSI Design, Term 071
HW# 3

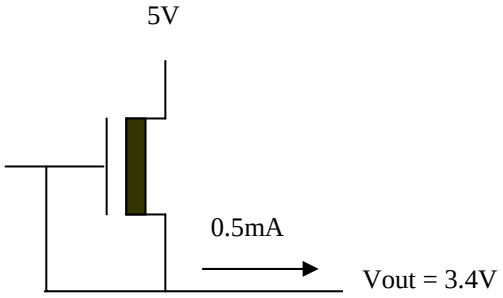
Q.1. Assuming nMOS enhancement transistor threshold voltage V_{tn} of 1.0 V, depletion transistor threshold voltage V_{td} of -2.0 V, and pMOS enhancement transistor threshold voltage V_{tp} of -1.0 V, write down the voltages of the indicated nodes below. Assume that the body effect is negligible.



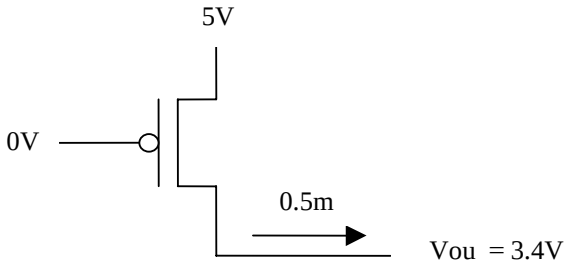
Q.2. It is required to design a pull-up MOS transistor that should be able to deliver a current of 0.5 mA while the output voltage is maintained at 3.4 volts (see the figures below). If the transistors use the minimum channel length of 1.0μ and a minimum grid size of 0.25μ, calculate the minimum width of such a transistor if the used transistor is:

(i) Depletion-type NMOS transistor with μC_{ox}=200 uA/v^2, V_{td} =-2.0 v, γ=0.5 $v^{1/2}$, $2\phi_b$ = 0.6 v.

(ii) PMOS transistor with μC_{ox}=40 uA/v^2, V_{tp}=-1.0 v, γ=0.5 $v^{1/2}$, $2\phi_b$ = 0.6 v.



Depletion NMOS Pull Up



PMOS Pull

Q.3. An NMOS transistor is measured to have a drain current of 2mA at V_{GS}=V_{DS}=9v, and of 0.5 mA at V_{GS}=V_{DS}=5v. Determine the values of β and V_{tn} for the transistor.