

HW#2

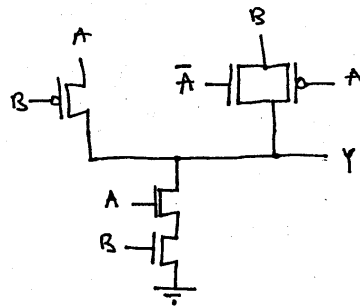
Q1 (i)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$$\Rightarrow Y = \bar{A}B + A\bar{B} = A \oplus B$$

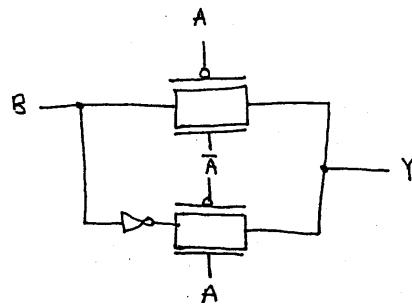
(ii) The problem with this implementation is that for the input combination $A=0$ & $B=0$ does not produce a good 0, i.e. 0 volt. The output Y will be discharged to $|V_{tp}|$ and then the pmos transistors will turn off.

One solution to overcome this problem is shown below:



In this implementation, when $A=0$ & $B=0$, the output Y will discharge completely to 0 volts because of the nmos transistor controlled by \bar{A} .

(iii) Transmission gate implementation:

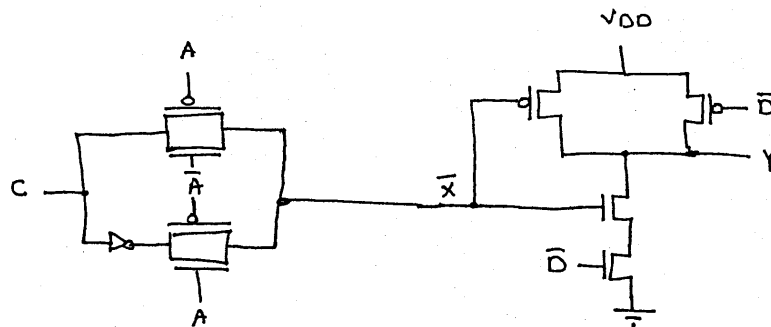


Q2

$$\begin{aligned} \text{(i)} \quad Y &= \bar{A}\bar{C} + \bar{A}D + AC + AD \\ &= \underbrace{\bar{A}\bar{C} + AC}_{\text{XNOR}} + D \end{aligned}$$

$$\text{Let } X = \bar{A}\bar{C} + AC \Rightarrow Y = X + D$$

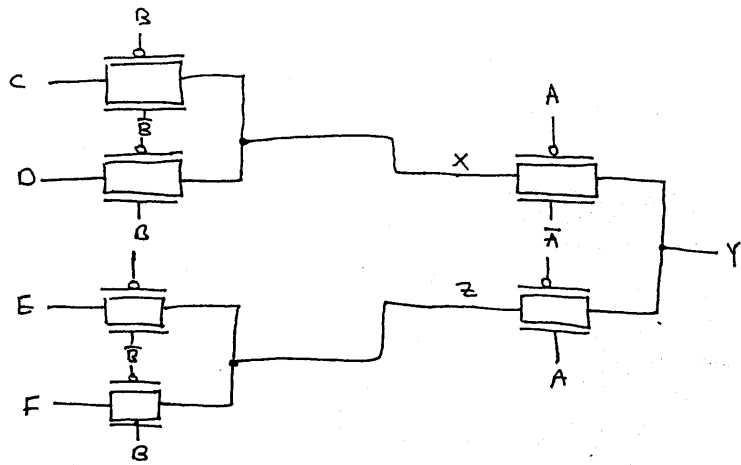
$$\bar{Y} = \bar{X}\bar{D}, \quad \bar{X} = \bar{A}C + A\bar{C}$$



$$\begin{aligned} \text{(ii)} \quad Y &= \bar{A}\bar{B}C + \bar{A}BD + A\bar{B}E + ABF \\ &= \bar{A} \underbrace{[\bar{B}C + BD]}_{\text{MUX}} + A \underbrace{[\bar{B}E + BF]}_{\text{MUX}} \end{aligned}$$

$$\text{Let } X = \bar{B}C + BD \quad \text{and} \quad Z = \bar{B}E + BF$$

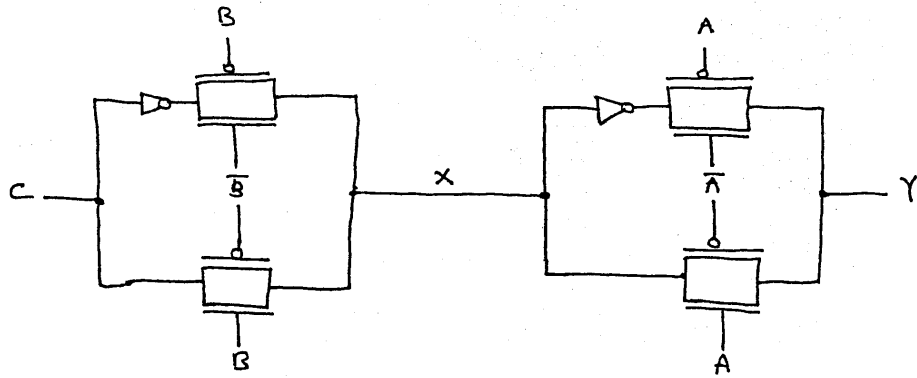
$$\Rightarrow Y = \underbrace{\bar{A}X + AZ}_{\text{MUX}}$$



$$\begin{aligned}
 \text{(iii)} \quad Y &= A\bar{B}\bar{C} + \bar{A}B\bar{C} + ABC + \bar{A}\bar{B}C \\
 &= A \underbrace{[\bar{B}\bar{C} + BC]}_{\text{XNOR}} + \bar{A} \underbrace{[B\bar{C} + \bar{B}C]}_{\text{XOR}}
 \end{aligned}$$

$$\text{Let } X = \bar{B}\bar{C} + BC, \quad \bar{X} = B\bar{C} + \bar{B}C$$

$$\Rightarrow Y = \underbrace{AX + \bar{A}\bar{X}}_{\text{XNOR}}$$



Q3 (i) $Y = \bar{A}C + \bar{B}D$

(ii) Let us call the first part of the circuit X.

Then, $X = \bar{A}\bar{B}$

$$\begin{aligned} \Rightarrow Y &= XC + \bar{X}D \\ &= \bar{A}\bar{B}C + (A+B)D \\ &= \bar{A}\bar{B}C + AD + BD \end{aligned}$$

Q4 Falling-edge DFF

