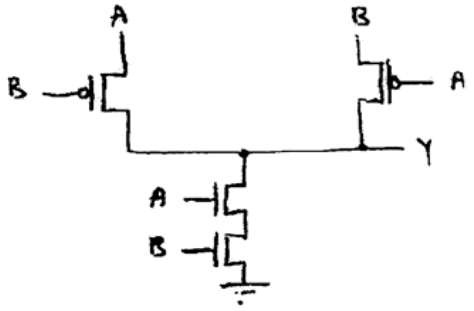
COE 360, Principles of VLSI Design, Term 71
HW# 2

Q.1. Consider the transistor-level implementation of the 2-input gate shown below. Assume that the threshold voltages of the nMOS and pMOS transistors are V_{tn}=1v and V_{tp}=-1v.



(a) Determine the function implemented by the gate.

(b) Is there any problem with the given implementation? If there is a problem, then suggest a modification to the implementation to overcome the problem.

(c) Reimplement the gate function using only transmission gates and inverters.

Q.2. Implement the following in CMOS using the smallest possible number of transistors assuming the availability of inverted inputs:

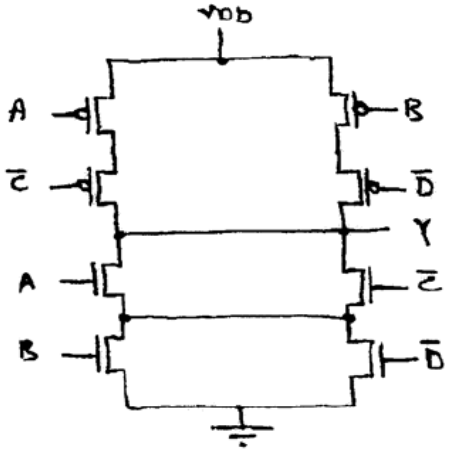
(a) $Y = A'C' + A'D + AC + AD$

(b) $Y = A'B'C + A'BD + AB'E + ABF$

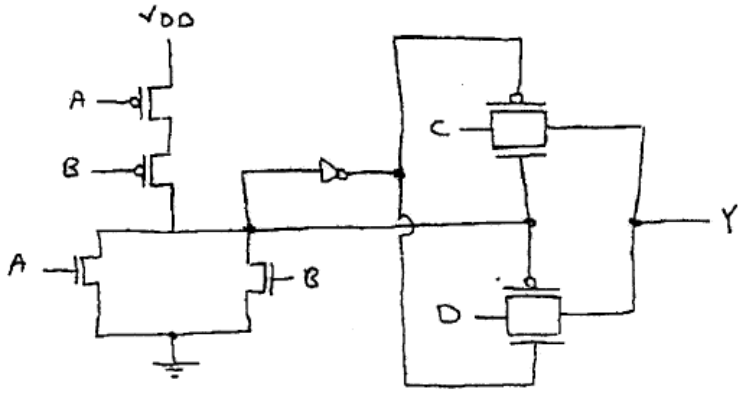
(c) $Y = AB'C' + A'BC' + ABC + A'B'C$

Q.3. Express the functions implemented by the following gates:

(a)

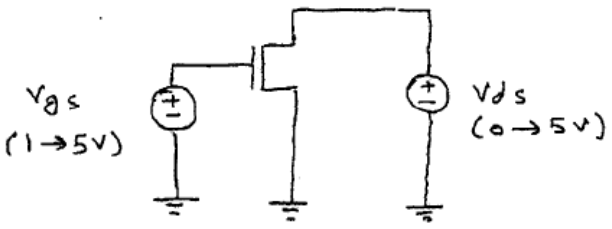


(ii)



Q.4. Design a falling-edge D-flip flop using CMOS gates.

Q.5. Consider an nMOS transistor with a threshold voltage V_m=1v, L=1u, and W=2u, as shown below.



(i) Using spice, draw the voltage-current graph by changing Vgs from 1v to 5v, and Vds from 0v to 5v.

(ii) Redraw the voltage-current graph by changing W to 20u. What are your observations?