

Principles of VLSI Design COE 360 (3-0-3)

Course Description

Instructor

Dr. Aiman El-Maleh

Room 22-332

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Office Hours

SMW 10:00-11:00

SW 1:30-3:00

Or by appointment

Catalog Description

MOS Transistor operation and limitations, MOS digital logic circuits (NMOS & CMOS), static & dynamic logic, combinational and sequential circuits, propagation delay, transistor sizing, MOS IC fabrication, layout and design rules, stick diagrams, IC Design and Verification Tools, subsystem design and case studies, and practical considerations.

Prerequisite: EE 203

Text Book: N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design*, Addison Wesley, 1993.

Topics:

1. ***Review Material:*** Semiconductor types and dopings, Mobility and Conductivity. Mass-action-Law, Charge-Neutrality-Law. Drift and Diffusion currents in semiconductors, Open Circuit P-N junction, built-in Potential, Space Charge Transition Capacitance, PN-junction breakdown. Basic Specifications of Digital Circuits (V_{OL} , V_{OH} , V_{IL} , V_{IH} , I_{OL} , I_{OH} , I_{IL} , I_{IH} , Noise Margin, Fanin, Fanout and loading, Power dissipation,
2. ***The MOS Transistor:*** Structure and operation. Threshold voltage, body effect, I-V characteristics and second order effects, MOS capacitances, SPICE MOS model parameters.
3. ***CMOS Processing Technology,*** Photolithography, masking and etching. CMOS fabrication. CMOS design rules and layout, CMOS Latchup. Sheet resistance, integrated resistors, and capacitors. Distributed RC Effect, Scaling of MOS circuits.
4. ***MOS Static Logic.*** Static NMOS & CMOS logic, NMOS pass transistors, CMOS transmission gates, inverter delay models, transistor sizing, and power dissipation in MOS circuits, Latches and registers.
5. ***CMOS Dynamic & Other Logic:*** Pseudo NMOS logic, clocked logic, domino logic, pass transistor logic.
6. ***CMOS Subsystem Design & Case Studies.*** Design of CLA Adder, shifter, ALU, decoders, counters, SRAM cells, case studies.

Grading Policy

<i>Assignments</i>	10 points
<i>Quizzes</i>	10 points
<i>Project</i>	15 points
<i>Exam I (October 17)</i>	20 points
<i>Exam II (November 21)</i>	20 points
<i>Final Exam</i>	25 points
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Total	100 points

Attendance Policy

Attendance will be taken regularly,

A 0.5 percentage point will be deducted for every unexcused absence,

Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.