COMPUTER ENGINEERING DEPARTMENT
COE 360 Principles of VLSI Design
Syllabus – Term 032

Instructor
Dr. Aiman El-Maleh **Room** 22-318 **Phone**: 2811 **e-mail**: aimane@ccse

Catalog Description

MOS Transistor operation and limitations, MOS digital logic circuits (NMOS & CMOS), static & dynamic logic, combinational and sequential circuits, propagation delay, transistor sizing, MOS IC fabrication, layout and design rules, stick diagrams, IC Design and Verification Tools, subsystem design and case studies, and practical considerations.

Prerequisite: EE 203.

Text Book: S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 2nd ed., 1999.

Reference: N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design*, Addison Wesley, 1993.

Course URL: www.ccse.kfupm.edu.sa/~aimane/coe360

Topics:

1. ***Review Material:*** Semiconductor types and dopings, Mobility and Conductivity. Mass-action-Law, Charge-Neutrality-Law. Drift and Diffusion currents in semiconductors, P-N junction, built-in Potential, Transition Capacitance, and breakdown voltage. Basic Specifications of Digital Circuits (V_{OL}, V_{OH}, V_{IL} , V_{IH}, I_{OL}, I_{OH}, I_{IL}, I_{IH}, Noise Margin, Fanin, Fanout and loading, Power dissipation).
2. ***The MOS Transistor:*** Structure and operation. Threshold voltage, body effect, I-V characteristics and second order effects, MOS capacitances, SPICE MOS model parameters, SPICE simulations.
3. ***CMOS Processing Technology:*** Photolithography, masking and etching. CMOS fabrication. CMOS design rules and layout. CMOS Latchup. Sheet resistance, integrated resistors, and capacitors. Distributed RC Effect.
4. ***MOS Static Logic:*** Static NMOS & CMOS logic, NMOS pass transistors, CMOS transmission gates, inverter delay models, transistor sizing, and power dissipation in MOS circuits, Latches and registers.
5. ***CMOS Dynamic & Other Logic:*** Dynamic CMOS Logic (Precharge/Evaluate), Charge Sharing, Domino logic, NORA CMOS logic, True Single-Phase Clock (TSPC) logic.
6. ***CMOS Subsystem Design & Case Studies***: Design of CLA Adder, shifter, ALU, decoders, counters, SRAM cells, case studies.
7. ***Second-Order Considerations:*** MOS transistor scaling, Small geometry & second order effects.
8. ***VLSI Design Styles***: Custom vs. Semicustom techniques, Standard Cells, Gate Arrays, and FPGAs.

Grading Policy

Hws &Quizzes	15 points
Project	20 points
Exam I	20 points
Exam II	20 points
Final Exam	25 points
Total	100 points

Attendance Policy

Attendance will be taken regularly,
Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.