January 1, 2008

COMPUTER ENGINEERING DEPARTMENT

COE 360

PRINCIPLES OF VLSI DESIGN

Major Exam II

First Semester (071)

Time: 7:00-9:30 PM

Student Name : _____

Student ID. : _____

Question	Max Points	Score
Q1	15	
Q2	15	
Q3	20	
Q4	15	
Q5	35	
Total	100	

Dr. Aiman El-Maleh

[15 Points]

(Q1)

(i) A basic n-well CMOS fabrications process involves a sequence of processing steps. **Order the steps** given below, used in a basic n-well CMOS fabrications process, in the right order:

- Metal1 mask
- Metal2 mask
- Contact cut mask
- N-well mask
- Channel stop implant
- Active mask
- N+ mask
- Polysilicon mask
- P+ mask
- Local Oxidation of silicon

(ii) During the CMOS fabrication process, parasitic MOS transistors get created between unrelated transistors. Discuss how it can be guaranteed that these parasitic MOS transistors will not affect the circuit operation.

(iii) A cross-sectional view of a single-metal N-Well CMOS process is shown below. Fill in the table giving the corresponding layer name Label (A, B, …N).

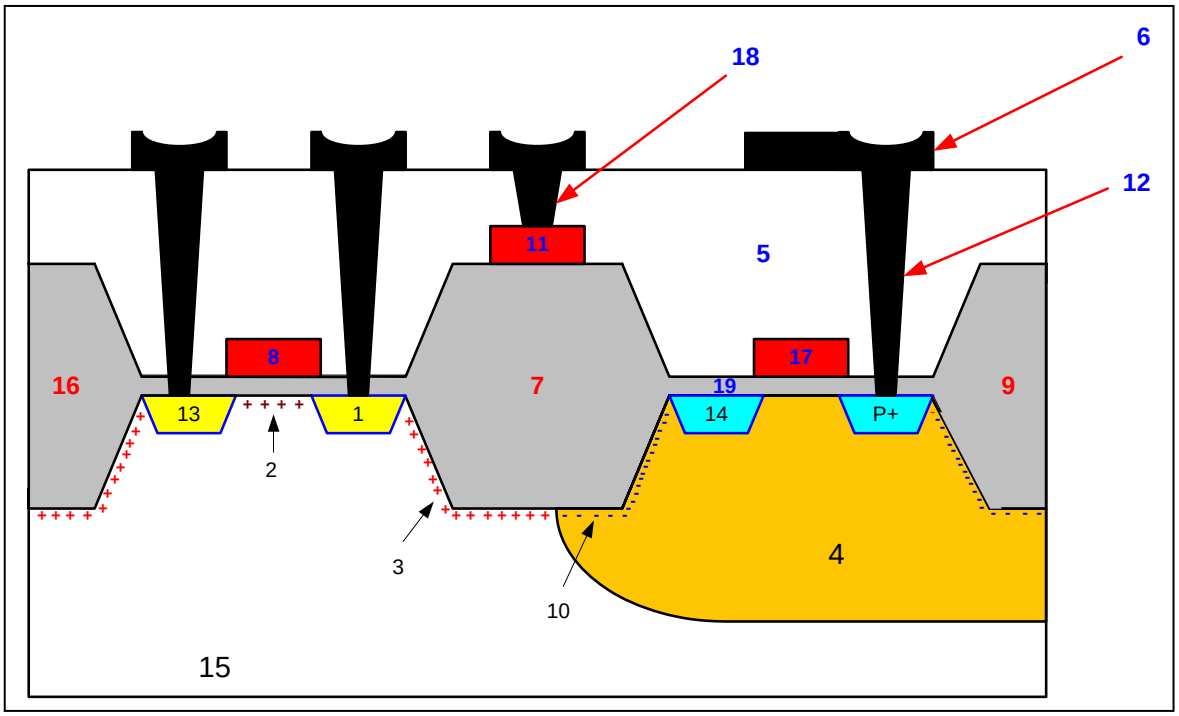


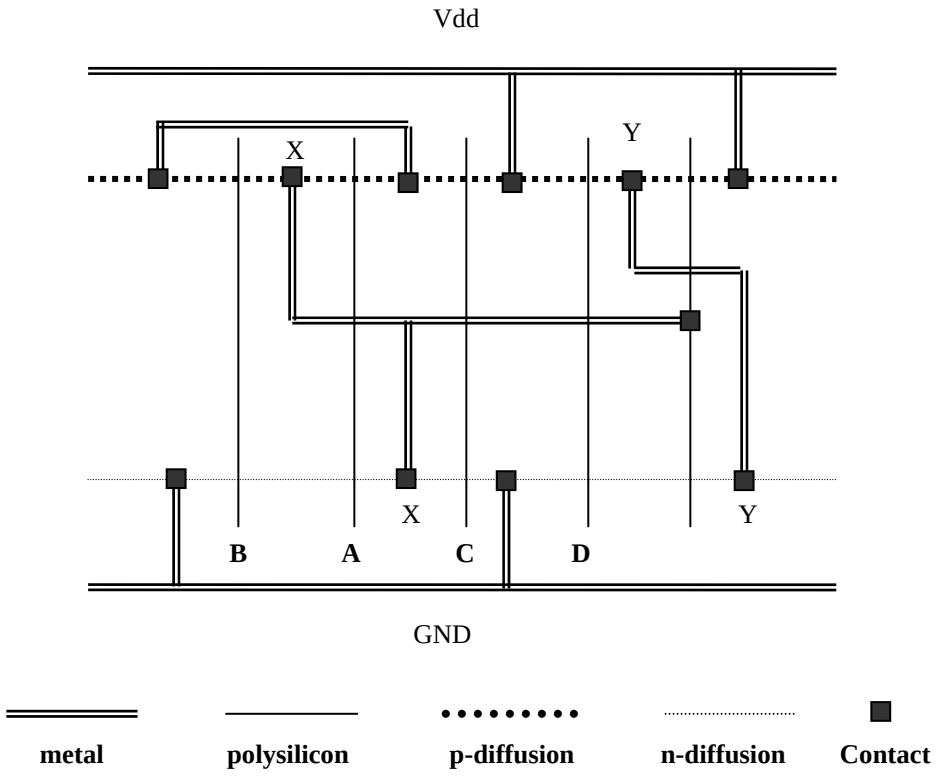
Figure Label	Layer Name Label (A,B →N)
1	
2	
3	
4	
5	
6	
7	
8	
10	
12	
14	
15	
18	
19	

Layer Name Labels

A. P-Substrate
B. N-Well
C. P-Field Implant
D. N-Field Implant
E. Field Oxide
F. Thin Oxide
G. Passivation Oxide
H. VT-adjust Implant
I. Poly Gate
J. Poly Interconnect
K. N+ Implant (N-Select)
L. P+ Implant (P-Select)
M. Metal
N. Contact Cut

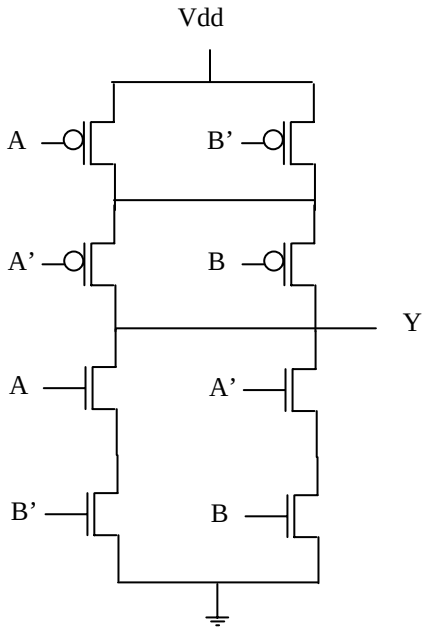
[15 points]

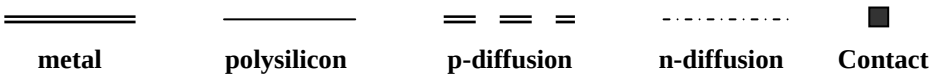
(Q2) Given the stick-diagram layout shown below, implementing the function Y=F(A,B,C,D), extract the transistor-level circuit corresponding to the layout and determine the function it implements.



[20 points]

(Q3) Draw the **stick diagram layout** of the transistor-level circuit shown below using **one metal layer**. Show the n- and p-networks, and the Euler paths you identify. **Minimize the wire lengths and the contact cuts** used. **Do not change the structure of the circuit**. **Do not assume the availability of inverted inputs**. You can use the legend given below for representing the different layers.





[15 points]

(Q4) Consider the spice model given below. Determine the **transistor-level circuit** modeled. What is the function modeled by this circuit? Plot the waveforms that will be generated by the .plot command for v(1), v(2) and approximate sketch of v(7).

```
* Test Circuit
.subckt gate1 1 2 3 4
m2 3 2 4 4 pfet w=2u l=1u
m1 3 2 1 1 nfet w=1u l=1u
.ends

.subckt gate2 1 2 3 4 5 6
M1 1 2 4 6 pfet w=2u l=1u
M2 1 3 4 5 nfet w=1u l=1u
.ends

vcc 5 0 5v

v1 1 0 pulse (0 5 20ns 2ns 2ns 15ns 35ns)
v2 2 0 pulse (0 5 10ns 2ns 2ns 20ns 50ns)

X1 0 2 3 5 gate1
X2 1 3 2 4 0 5 gate2
X3 0 4 6 5 gate1
X4 0 6 7 5 gate1
X5 7 2 3 4 0 5 gate2
c1 7 0 0.5pf

.model nfet nmos (vto=1.0 KP=80u)
.model pfet pmos (vto=-1.0 KP=40u)

.nodeset v(7)=0
.tran 0.1ns 100ns
.plot tran v(1) v(2) v(7)
.end
```

[35 points]

(Q5) Consider the depletion-load circuit shown below with the following parameters: V_{tn}=1.0 V, V_{td}=-3.0 V, $\mu_n C_{ox}$=100 uA/V^2, V_{DD}=5 V, γ=0.4 $V^{1/2}$, $|-2\phi_f|$ = 0.6 V, and $(W/L)_{load}$=1/3. Assume that the enhancement NMOS transistors use the minimum channel length of 1.0μ and a minimum grid size of 0.1μ.

1. Show that for a depletion-load inverter

$$V_{OL} = V_{OH} - V_{tn} - \sqrt{(V_{OH} - V_{tn})^2 - \left(\frac{\beta_{load}}{\beta_{driver}}\right) |V_{td}(V_{OL})|^2}$$

2. Design the circuit (i.e., determine the W/L ratios of the nmos transistors) such that the **worst case V_{OL}=0.2V**. Use the minimum possible area to achieve the requirement.
3. Compute the **lowest V_{OL}** achieved by the designed circuit.
4. Calculate the **maximum DC power** dissipated by the circuit.

Note that: $V_T(V_{SB}) = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$ and $\gamma = \frac{\sqrt{2qN_A\varepsilon_{si}}}{C_{ox}}$