**Nov. 4, 2007**

# COMPUTER ENGINEERING DEPARTMENT

## COE 360

## PRINCIPLES OF VLSI DESIGN

**Major Exam I**

**First Semester (071)**

**Time: 7:30-9:30 PM**

Student Name : ______________________________________________

Student ID.   : ______________________________________________

| Question | Max Points | Score |
| --- | --- | --- |
| I | 26 | |
| II | 15 | |
| III | 13 | |
| IV | 16 | |
| V | 16 | |
| VI | 14 | |
| Total | 100 | |

Dr. Aiman El-Maleh

# FORMULA SHEET

$E_g$ *(Silicon Energy Gap)* $= 1.1\,ev$
*q (Electron charge) = 1.6 x* $10^{-19}$ *Coulombs*
$\varepsilon_{ox}$ *(Permittivity of Oxide) =0.34 x* $10^{-12}$ *F/cm*
$\varepsilon_{si}$*(Permittivity of Silicon) = 1.06 x* $10^{-12}$ *F/cm*
$n_i$ *(Silicon intrinsic concentration at Room Temperature) = 1.5 x* $10^{10}$ $cm^{-3}$
$\mu_n$ *( Electron mobility at Room Temperature) =600* $cm^2/V.s$
$\mu_p$ *( Hole mobility at Room Temperature) =250* $cm^2/V.s$

$$V_{bi} = \frac{KT}{q}\ln\frac{N_A N_D}{ni^2}$$

$$\phi_{Fp} = \frac{KT}{q}\ln\frac{n_i}{N_A}$$

$$\phi_{Fn} = \frac{KT}{q}\ln\frac{N_D}{n_i}$$

$$\frac{KT}{q} = 0.025v \text{ (at Room Temperature)}$$

$$\text{Workfunction } q\Phi_S = q\chi + (E_c - E_F)$$

$$Q_B = -\sqrt{2q.N_A.\varepsilon_{si}.|\phi_F - \phi_S|}$$

$$x_d = \sqrt{\frac{2\varepsilon_{si}.|\phi_F - \phi_S|}{q.N_A}}$$

$$V_T(V_{SB}) = V_{T0} + \gamma(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|})$$

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_{si}}}{C_{ox}}$$

**[26 Points]**

**(I) Indicate whether the following is true or false, and if it is false <u>briefly describe why it is false:</u>**

1. **(True, False)** In a p-type semiconductor, electrons contribute larger current compared to holes since electron mobility is larger than hole mobility.

2. **(True, False)** In an intrinsic silicon semiconductor, at T=0 K, the valence electrons are distributed equally between the valence energy band and the conduction energy band.

3. **(True, False)** The Fermi-level for both n-type and p-type transistors is above the intrinsic Fermi level.

4. **(True, False)** For both nmos and pmos transistors, the substrate (body) is connected to ground and current flows from the source to drain.

5. **(True, False)** The concentration of free electrons in an n-type semiconductor, $n = ni^2/p$.

6. **(True, False)** In general, higher doping concentrations result in lower depletion region width and lower transition capacitance.

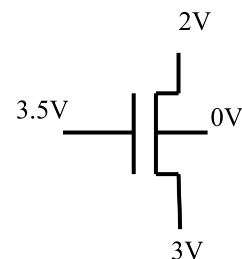
7. **(True, False)** The width of the depletion region in a forward-biased pn junction is wider than that of a reverse-biased pn junction.

**8.** **(True, False)** The higher the doping concentrations of the pn junction are the lower the magnitude of the built-in electric field and the higher the breakdown voltages.

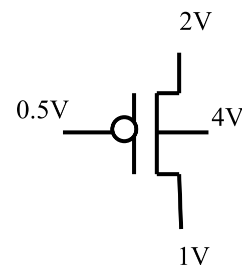
**9.** **(True, False)** In an n-type silicon semiconductor, increasing the doping concentration increases the Fermi level towards the conduction band and increases the Fermi potential.

**10.** **(True, False)** The value of the threshold voltage of an nmos transistor increases with increasing the doping concentration of the substrate, increasing the gate oxide thickness, increasing impurities in Si-Oxide interface, increasing temperature and with increasing the voltage difference between the source and substrate.

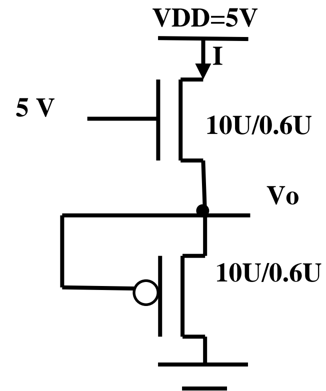
**11.** **(True, False)** The enhancement NMOS transistor shown has a threshold of 0.8V, with the shown terminal voltages. This transistor is in Linear region**.**



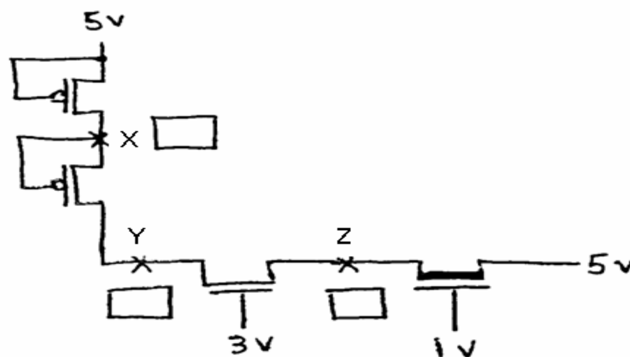

**12.** **(True, False)** The enhancement PMOS transistor shown has a threshold of -0.8V, with the shown terminal voltages. This transistor is in Saturation region**.**



**13. (True, False)** Assume that for the enhancement MOSFETs Vtn=│Vtp│=0.8V, Cox = 2 fF/$\mu m^2$ (i.e. 2E-7 F/$cm^2$), $\mu_n$ = 600 and $\mu_p$ = 300. For the circuit shown below, the value of I is approximately 0.149 mA and the value of Vo is approximately 0.8 v.



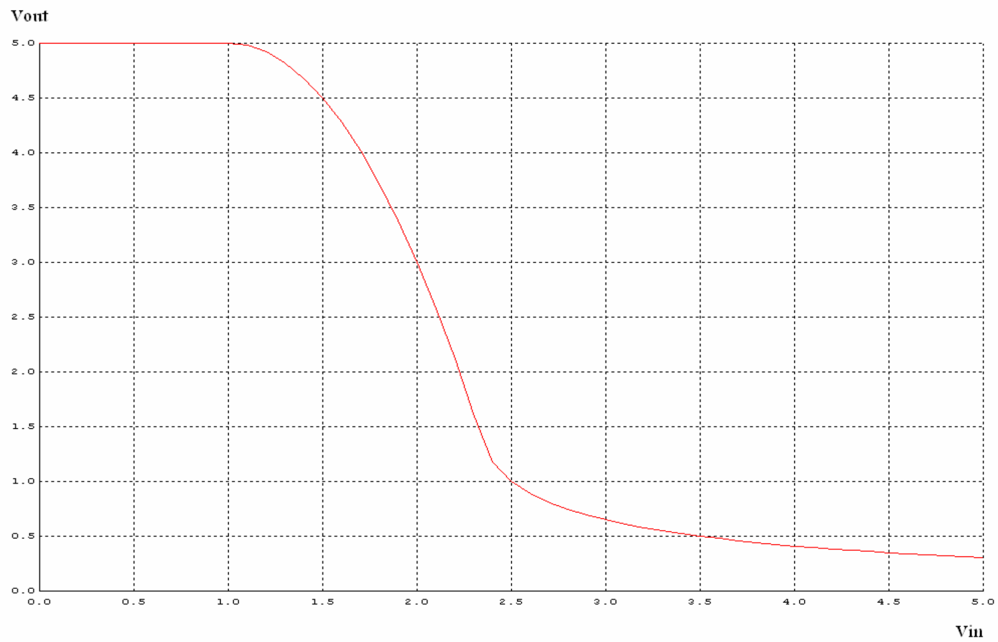

**14. (True, False)** Assuming nMOS enhancement transistor threshold voltage $V_{tn}$ of 1.0 V, depletion transistor threshold voltage $V_{td}$ of -2.0 V, and pMOS enhancement transistor threshold voltage $V_{tp}$ of -1.0 V, and assuming that the body effect is negligible, the voltage at node X is 1 V, the voltage at node Y is 2 V and the voltage at node Z is 3 V.

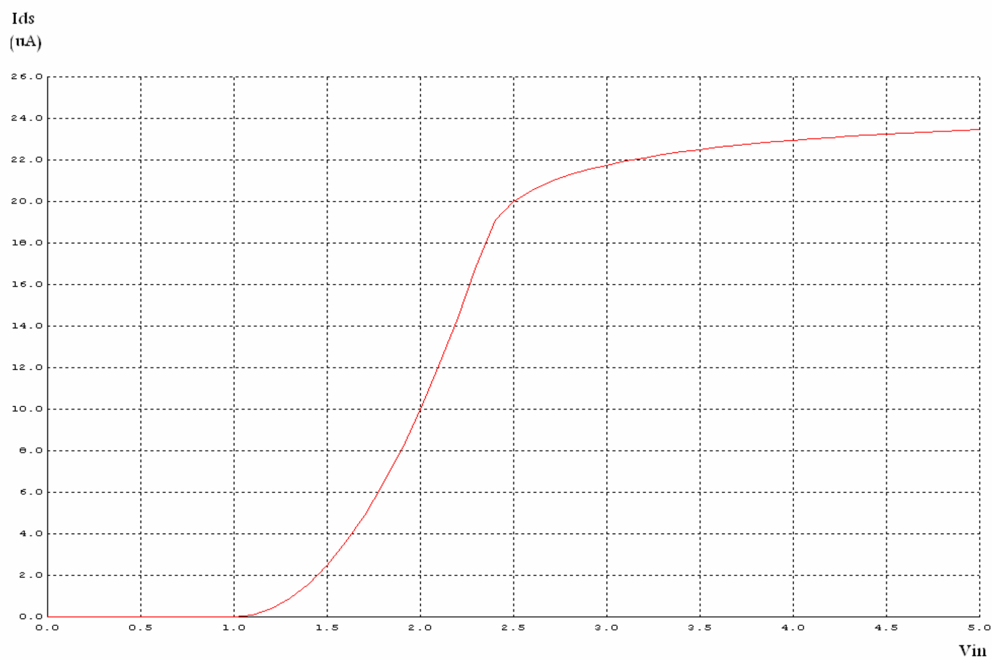


**[15 Points]**

**(II)** Given below is the Voltage Transfer Characteristic and Voltage-Current Characteristic of a **Resistive-Load Inverter**.

1. Determine $\mathbf{V_{tn}}$, $\mathbf{V_{OH}}$, $\mathbf{V_{OL}}$, $\mathbf{V_{IH}}$, $\mathbf{V_{IL}}$, **NMH, NML** of the inverter.
2. Under what value of the input, the resistance of the NMOS transistor is equal to the resistance of the pullup resistor. Justify your answer.
3. Determine the value of the pullup **resistor**.
4. Dtermine the **Average DC Power** dissipation for this inverter.



**[13 Points]**

**(III)** The piece of silicon shown below is originally of **P-type** and has a resistivity of 20 Ω.cm.

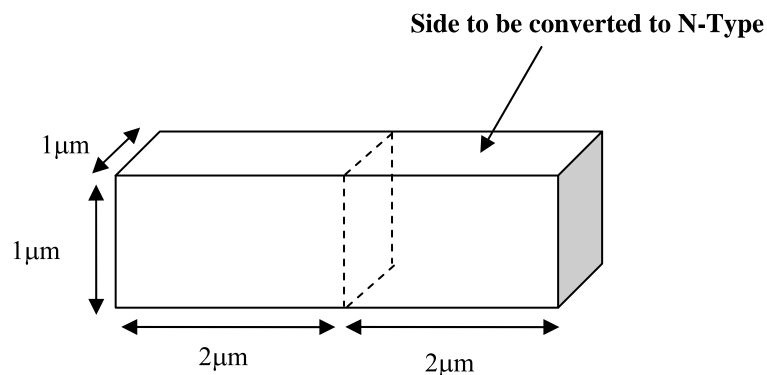
**1.** Determine the **acceptor concentration** in this piece of silicon.

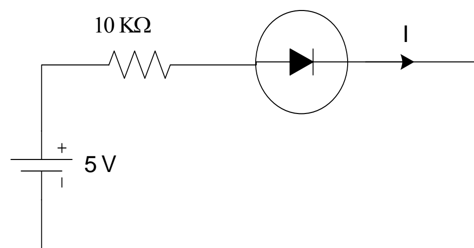
**2.** Determine the **donor concentration** required to convert one side of this piece of silicon to N-type with a resistivity of 5 Ω.cm.

**3.** Calculate the **built-in potential** of this junction.

**4.** Calculate the **series resistance** of this junction.

**5.** If the resulting P-N junction is used in the circuit shown below, calculate the value of the **current I.**

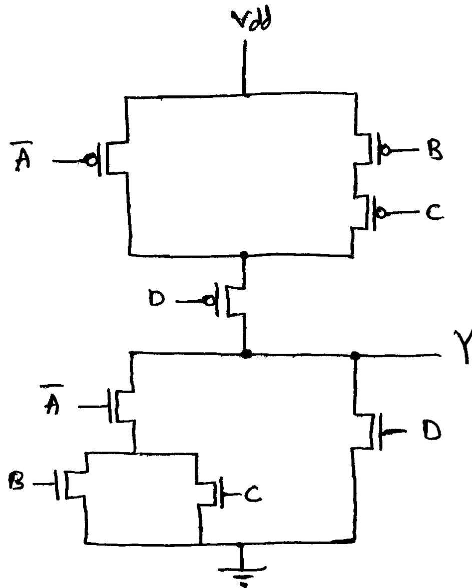


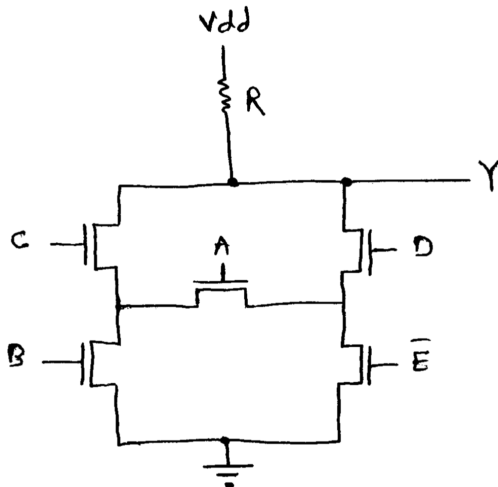
**[16 points]**

**(IV)** Determine the function implemented by each of the following circuits:

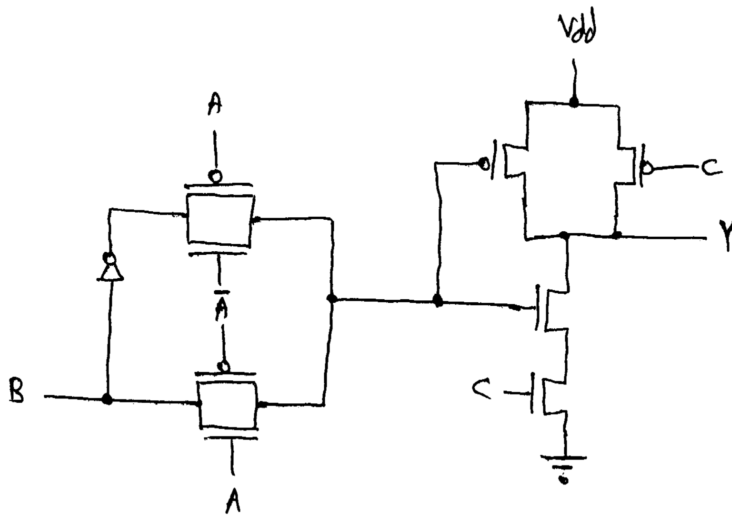
**1.**



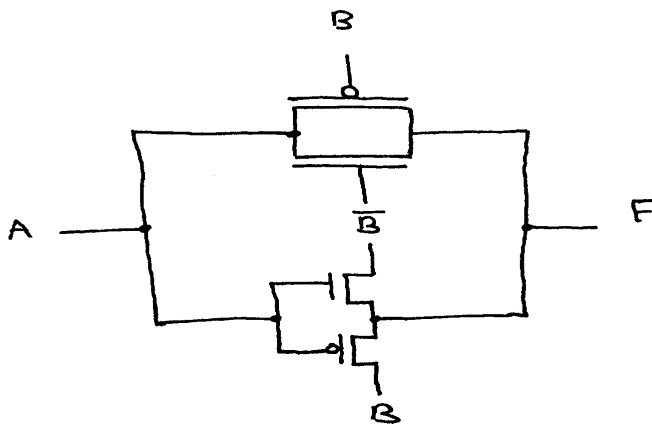

**2.**



**3.**




**4.**



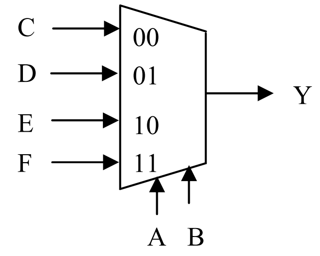
**[16 points]**

**(V)** Implement the following functions in **CMOS** using the **smallest possible number of transistors**. Note that you can use transmission gates in your implementation. Indicate the total number of transistors used in each implementation. Assume that the given sum-of-products expressions are minimal, i.e. **no two-level minimization is required**.

1. **Y = [ (A + B C') (D + E') ]**

2. **Y = [A B C + A' B' C + A' B D + A B' D]'**

**3.** The **4X1 multiplexer** shown below.




**4.** An **active high D-Latch with asynchronous active-high Reset** input, i.e. if Reset=1, Q=0 independent of the clock.

**[14 points]**

**(VI)** A set of *I-V* characteristics for an **nMOS** transistor at room temperature is shown below for different biasing conditions. Assume that $|2\phi_F|=0.6$ and $\gamma = 0.36\,\text{v}^{1/2}$ and that the effect of channel-length modulation can be ignored.

| $V_{GS}\,(v)$ | $V_{DS}\,(v)$ | $V_{SB}\,(v)$ | $I_D\,(\mu A)$ |
|---|---|---|---|
| 3 | 3 | 0 | 97 |
| 4 | 4 | 0 | 235 |
| 5 | 5 | 0 | 433 |
| 4 | 4 | 3 | 173 |

1. Determine the transistor threshold voltage $V_{T0}$, and the transconductance, $k_n$ ($\beta_n$).
2. Determine the current that flows across the transistor when $V_G$=5V, $V_D$=2V, and $V_S$=1V.