KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 360 Principles of VLSI Design
Term 991 Lectures

	Date	Topics	Ref.
1	M 6/09	Syllabus. Introduction.	1.6 &1.7
2	W 8/09	*Conduction in metals, current density, mobility and conductivity, drift current, intrinsic semiconductors, extrinsic semiconductors.*	Notes
3	S 11/09	*N-type and p-type semiconductors, mass-action-law, charge-neutrality law, diffusion current, open-circuit P-N junction, built-in potential.*	Notes
4	M 13/09	*Forward and reverse-biased P-N junctions, transition capacitance, P-N junction breakdown.*	Notes
5	W 15/09	*Basic specifications of digital circuits (V_{OL}, V_{OH}, V_{IL}, V_{IH}, noise margin, fanin, fanout, loading, and power dissipation).* **(HW#1 Distributed**)	2.3.2, notes
6	T 16/09	*Structure of nmos and pmos transistors, transmission gate, inverter, nand, and nor gates.*	1.3, 1.4, 1.5, notes
7	S 18/09	*Compound gates, multiplexers, xor and xnor gates, D-latch and D-FF.*	1.5, notes
8	M 20/09	*MOS transistor theory: structure and operation, threshold voltage.* **(HW#1 Collected**)	2.1, notes
9	W 22/09	*MOS device design equations.* **(Quiz#1)**	2.2, notes
10	S 25/09	*Threshold voltage body effect, channel-length modulation, drain punchthrough, impact ionization, spice DC parameters.* **(HW#2 Distributed**)	2.2, notes
11	M 27/09	*Types of MOS transistors: enhancement- and depletion-types. Summary of operation regions of MOS transistors.*	2.3, notes
12	W 29/09	*CMOS processing technology: oxidation, epitaxy, deposition, ion implantation, diffusion, patterning of SiO_2, fabrication steps for a silicon gate nmos transistor, parasitic MOS transistor.*	3.1, notes
13	S 2/10	*CMOS n-well process, substrate and well contacts, multiple metal layers, p-well process, twin-well CMOS process, layout design rules.* **(HW#2 Collected**)	3.2, 3.4, notes
14	M 4/10	*The latch-up problem.* **(Quiz#2)**	3.5, notes
15	W 6/10	*Layout design of simple logic gates: inverter, NAND, and NOR. Complex gates layout.*	5.3, notes
16	S 9/10	*Complex gates layout: examples.* **(HW#3 Distributed**)	5.3, notes
17	M 11/10	*Resistive-load inverter: calculation of V_{OL}, V_{OH}, V_{IL}, V_{IH}.*	2.4, notes
18	W 13/10	*Resistive-load inverter: calculation of V_{th}. Voltage transfer characteristic, power consumption.*	2.4, notes

19	S 16/10	*Review for Exam I.* **(HW#3 Collected**)	
	U17/10	**EXAM I**	
20	M 18/10	*Saturated Enhancement-load inverter: calculation of V_{OL}, V_{OH}, V_{IL}, V_{IH}.*	2.4, notes
21	W 20/10	*Linear Enhancement-load inverter, pseudo-nmos inverter.*	2.4, notes
22	S 23/10	*Depletion-type nmos load inverter: calculation of V_{OL}, V_{OH}, V_{IL}, V_{IH}. voltage transfer characteristic, power consumption.*	Notes
23	M 25/10	*CMOS inverter: calculation of V_{OL}, V_{OH}, V_{IL}, V_{IH}.*	2.3, notes
24	W 27/10	*CMOS inverter: calculation of V_{th}. Voltage transfer characteristic, power consumption*. Design of CMOS inverters. **(HW#4 Distributed**)	2.3, notes
25	S 30/10	*Inverter-equivalent circuits: Nand and Nor gates.*	Notes
26	M 1/11	*Inverter-equivalent circuits: Compound gates.*	Notes
27	W 3/11	*Resistance estimation. Capacitance estimation*: MOS capacitor characteristics. **(HW#4 Collected**)	4.2, 4.3, notes
28	S 6/11	*MOS device capacitances, diffusion capacitance*. **(Quiz#3)**	4.3, notes
29	M 8/11	*Spice modeling of MOS capacitances, distributed RC effects.*	4.3, notes
30	W 10/11	*Capacitance estimation: Example.* **(HW#5 Distributed**)	4.3, notes
31	S 13/11	*Delay-time definitions: T_{PHL}, T_{PLH}, rising, and falling times.*	4.5, notes
32	M 15/11	*Calculation of delay times.*	4.5, notes
33	W 17/11	*Calculation of delay times.* **(HW#5 Collected**)	4.5, notes
34	S 20/11	*Review for Exam II.*	
	U 21/11	**EXAM II**	
35	M 22/11	*Power Dissipation: static dissipation, short-circuit* dissipation, and dynamic dissipation.	4.7, notes
36	W 24/11	*Total power dissipation estimation.*	4.7, notes
37	S 27/11	*Power dissipation estimation using the power meter technique*. **(HW#6 Distributed**)	notes
38	M 29/11	*Dynamic CMOS logic, cascading problem in dynamic CMOS logic.*	5.4, notes
39	W 1/12	*Domino CMOS logic, charge sharing problem.*	5.4, notes
40	S 4/12	*Measures to avoid erroneous output due to charge sharing, the Manchester carry chain.* **(HW#6 Collected**)	notes
41	M 6/12	*NORA CMOS logic*. **(Quiz#4)**	5.4, notes
42	W 8/12	*NORA CMOS logic, Zipper CMOS.*	5.4, notes
43	S 11/12	*Pass transistor logic.*	5.4, notes
44	M 13/12	*Scaling of MOS circuits.*	4.13, notes
45	W 15/12	Review for Final Exam.	