KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 360 Principles of VLSI Design
Term 043 Lecture Breakdown

	Date	Topics	Ref.
1	S 2/7	Syllabus. Introduction.	
2	U 3/7	VLSI system design process. Mobility, Current density, Drift and Diffusion, Conductivity, Resistivity.	Chapter 1, Handout
3	M 4/7	Semiconductors, Silicon atom, Covalent Bonds, Concept of a hole, Conduction and Valence bands. Intrinsic semiconductors, Extrinsic Semiconductors, Doners and Acceptors, n-type and p-type semiconductors. Mass Action Law, Fermi Energy. Charge neutrality law.	Handout
4	T 5/7	Fermi-level for n-type and p-type semiconductors, PN junction, depletion region. Forward-biased and reverse-biased PN junction.	Handout
5	W 6/7	Forward-biased and reverse-biased PN junction, Junction breakdown, Transition capacitance. Basic specifications of digital circuits: V_{OH}, V_{OL}, V_{IH}, V_{IL}, NMH, NML, V_{th}, fanin and fanout, power dissipation, propagation delay.	Handout
6	S 9/7	NMOS and PMOS transistors structure. NMOS and PMOS as pass transistors. Transmission gate. NMOS, PMOS and CMOS inverter. **(Quiz1)**	Handout
7	U 10/7	Implementation of logic gates in CMOS: NAND, NOR and general Boolean functions. Implementation of XOR, XNOR and 2x1 MUX using regular CMOS and transmission gates. Guidelines and examples for implementing general Boolean functions.	Handout
8	M 11/7	SR Latch implementation, Implementation of D-Latch & D-FF based on transmission gate. MOS transistor theory: accumulation, depletion and inversion modes, cutoff, saturation and linear regions.	Handout, Chapter 3
9	T 12/7	Operation regions of MOS transistor, Voltage-Current equations of MOS transistor. Enhancement and depletion type NMOS transistors.	Handout, Chapter 3
10	W 13/7	Fermi potential, work function, flatband voltage, the MOS system under external bias, Energy band diagrams of MOS under external bias. Threshold voltage.	Handout, Chapter 3
11	S 16/7	Fermi potential, work function, flatband voltage, the MOS system under external bias, Energy band	Handout, Chapter 3

		diagrams of MOS under external bias. Threshold voltage. **(Quiz#2)**	
12	U 17/7	Threshold voltage, Body bias effect, Measurement of parameters. Channel Length Modulation.	Handout, Chapter 3
13	M 18/7	Drain punch through, Impact ionization. Spice and WinSpice Tutorial.	Handout, Chapter 3
14	T 19/7	Spice and WinSpice Tutorial.	Handout
15	S 23/7	Solution of Exam I.	
16	U 24/7	Spice and WinSpice Tutorial. CMOS Processing technology: Silicon gate process, parasitic MOS transistor.	Handout, Chapter 2
17	M 25/7	Basic CMOS technology: Basic n-well CMOS process. Layout Design rules. Layout of CMOS Inverter and 2-input NAND gate.	Handout, Chapter 2 & 7
18	T 26/7	Layout of a 2-input NOR gate. Layout design of Transmission gate. Layout design strategy of any function.	Handout, Chapter 7
19	S 30/7	MAGIC Tutorial.	Handout
20	U 31/7	Resistive-load inverter: V_{OL}, V_{OH}, V_{IL}, V_{IH}, V_{th}. static power dissipation.	Chapter 5
21	M 1/8	Enhancement-Load Inverter: Saturated & Linear load inverters: V_{OH}, V_{OL}. **(Quiz#5)**	Chapter 5
22	T 2/8	No class.	
23	S 6/8	Depletion-Load Inverter: V_{OL}, V_{OH}, V_{IL}, V_{IH}, power dissipation. CMOS inverter: V_{OL}, V_{OH}, V_{IL}, V_{IH}, V_{th}, power dissipation.	Chapter 5
24	U 7/8	Inverter Equivalent Circuits. Pseudo-nmos inverter.	Handout, Chapter 5, 7
25	M 8/8	Delay time definitions, T_{PHL}, T_{PLH}, T_{rising}, $T_{falling}$. Calculation of delay times. Calculation of delay times. CMOS inverter design under delay constraints.	Chapter 6
26	T 9/8	Ring Oscillator Circuit. Resistance estimation. Capacitance Estimation: gate capacitance.	Handout, Chapter 6, 3, 7
27	S 13/8	Solution of Exam II.	
28	U 14/8	Junction capacitance. Source and drain capacitances. Spice modeling of capacitances. Interconnect capacitance. RC delay and design example.	Handout, Chapter 3
29	M 15/8	Load Capacitance of 2-input NAND and NOR gates. Dynamic power estimation. Power meter technique.	Chapter 6, 7
30	T 16/8	Power meter technique. Introduction to dynamic CMOS: Dynamic latch, Dynamic CMOS logic (precharge-evaluate), Domino Logic.	Chapter 6, 9
31	S 20/8	Charge sharing problem. Solutions to the charge-sharing problem. Manchester-Carry Chain Circuit. NORA logic. Examples of NORA logic.	Chapter 9
32	U 21/8	No Class.	

33	M 22/8		