KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 360 Principles of VLSI Design
Term 011 Lectures

	Date	Topics	Ref.
1	M 3/09	Syllabus. Introduction.	Chapter 1
2	W 5/09	VLSI system design process. Mobility, Current density, Conductivity, Resistivity.	Chapter 1, Handout
3	S 8/09	Semiconductors, Silicon atom, Covalent Bonds, Concept of a hole, Conduction and Valence bands.	Handout
4	M 10/09	Intrinsic semiconductors, Extrinsic Semiconductors, Doners and Acceptors, n-type and p-type semiconductors, Mass Action Law, Fermi Energy.	Handout
5	W 12/09	Charge neutrality law, Fermi-level for n-type and p-type semiconductors, PN junction, depletion region.	Handout
6	S 15/09	Forward-biased and reverse-biased PN junction, Junction breakdown, Transition capacitance.	Handout
7	M 17/09	Basic specifications of digital circuits: V_{OH}, V_{OL}, V_{IH}, V_{IL}, NMH, NML, V_{th}, fanin and fanout, propagation delay, power dissipation. NMOS transistor.	Handout
8	W 19/09	PMOS transistor. NMOS and PMOS as pass transistors. Transmission gate. NMOS, PMOS and CMOS inverter.	Handout
9	S 22/09	Implementation of logic gates in CMOS: NAND, NOR and general Boolean functions. (**Quiz#1**)	Handout
10	M 24/09	Implementation of XOR, XNOR and 2x1 MUX using regular CMOS and transmission gates. Guidelines and examples for implementing general Boolean functions.	Handout
11	W 26/09	Implementation of D-Latch & D-FF based on transmission gate. MOS transistor theory: accumulation, depletion and inversion modes, cutoff, saturation and liner regions, current-voltage equations.	Handout, Chapter 3
12	S 29/09	Fermi potential, work function, flatband voltage, the MOS system under external bias, Energy band diagrams of MOS under external bias.	Handout, Chapter 3
13	M 1/10	Threshold voltage, enhancement and depletion type NMOS transistors.	Handout, Chapter 3
14	W 3/10	Body bias effect, channel-length modulation, drain punchthrough, Impact ionization. Measurement of parameters.	Handout, Chapter 3
15	S 6/10	Example on NMOS transistor design. (**Quiz#2**)	Handout
16	M 8/10	CMOS Processing technology: oxidation, epitaxy, deposition, ion	Handout,

		implantation and diffusion, silicon gate process, parasitic MOS transistor.	Chapter 2
17	W 10/10	Basic CMOS technology: Basic n-well CMOS process. Layout of CMOS Inverter and 2-input NAND gate.	Handout, Chapter 2
18	S 13/10	N-well CMOS process, Layout Design rules. Layout of a 3-input NOR gate.	Handout, Chapter 2
19	M 15/10	Layout design of complex functions. Examples.	Handout, Chapter 7
20	W 17/10	Magic Tutorial.	Handout
21	S 20/10	Exam1 solution. Resistive-load inverter: V_{OL}, V_{OH}.	Chapter 5
22	M 22/10	Resistive-load inverter: V_{IL}, V_{IH}, V_{th}, static power dissipation.	Chapter 5
23	W 24/10	Enhancement-Load Inverter: Saturated & Linear load inverter. Depletion-Load Inverter: V_{OH}, V_{OL}, V_{IL}.	Chapter 5
24	S 27/10	Depletion-Load Inverter: V_{IH}. **(Quiz#3)**	Chapter 5
25	M 29/10	Depletion-Load Inverter: power dissipation. Pseudo-nmos inverter, CMOS inverter: V_{OL}, V_{OH}, V_{IL}, V_{IH}.	Chapter 5
26	W 31/10	CMOS inverter: V_{th}. Inverter Equivalent Circuits.	Handout, Chapter 5, Chapter 7
27	S 3/11	Inverter Equivalent Circuits. Resistance estimation.	Handout, Chapter 7
28	M 5/11	Capacitance Estimation: gate capacitance, junction capacitance.	Handout, Chapter 3
29	W 7/11	Source and drain capacitances. Spice modeling of capacitances.	Handout, Chapter 3
30	TH 8/11	Interconnect capacitance. RC delay and design example.	Handout
	S 10/11	No class.	
31	M 12/11	Delay time definitions, T_{PHL}, T_{PLH}, T_{rising}, $T_{falling}$. Calculation of delay times.	Chapter 6
32	W 14/11	Calculation of delay times. CMOS inverter design under delay constraints.	Chapter 6
33	S 17/11	Ring oscillator. Dynamic power estimation.	Chapter 6
34	M 19/11	Power meter technique.	Chapter 6
35	W 21/11	Dynamic latch. Dynamic CMOS logic (precharge-evaluate), Domino CMOS logic.	Chapter 9
36	S 24/11	Examples of Domino CMOS logic. Charge sharing problem. Solutions to the charge-sharing problem.	Chapter 9
37	M 26/11	Solution of Exam II.	
38	W 28/11	Manchester-Carry Chain Circuit. NORA logic.	Chapter 9
39	S 1/12	(**Quiz4**).	

40	M 3/12	NORA logic. Examples of NORA and DOMINO logic.	Chapter 9
41	W 5/12	Dynamic latches and flip-flops.	Chapter 9
42	S 29/12	Zipper CMOS circuits, Pipelined logic design using dynamic logic.	Chapter 9
43	M 31/12	MOS scaling: constant field scaling & constant voltage scaling. Latchup problem in CMOS.	Chapter 3
44	W 2/1	Latchup problem in CMOS.	Handout