Jan. 23, 2007

COMPUTER ENGINEERING DEPARTMENT

COE 360

PRINCIPLES OF VLSI DESIGN

Final Examination

First Semester (071)

Time: 7:30-10:30 AM

Student Name : _____

Student ID. : _____

Question	Max Points	Score
I	30	
II	10	
III	20	
IV	40	
Total	100	

Dr. Aiman El-Maleh

[30 points]

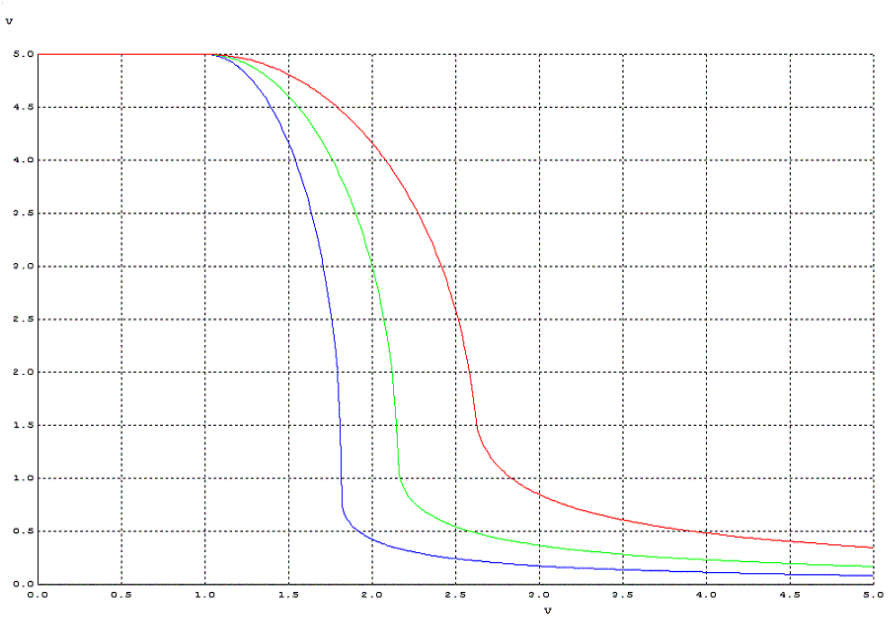
(I)

(1) Consider the spice model given below:

```
* Test Circuit1
.subckt g1 1 2
Vdd 5 0 dc 5
M1 2 1 0 0 nfet W=1u L=1u
M2 2 0 5 5 pfet W=1u L=3u
.ends

.subckt g2 1 2
Vdd 5 0 dc 5
M1 2 1 0 0 nfet W=2u L=1u
M2 2 0 5 5 pfet W=1u L=3u
.ends

.subckt g3 1 2
Vdd 5 0 dc 5
M1 2 1 0 0 nfet W=4u L=1u
M2 2 0 5 5 pfet W=1u L=3u
.ends


x1 1 2 g1
x2 1 3 g2
x3 1 4 g3

V1 1 0 DC

.dc V1 0 5 0.01

.model nfet nmos (vto=1.0 KP=80u)
.model pfet pmos (vto=-1.0 KP=40u)

.plot dc v(2) v(3) v(4)
.end
```

a. Draw the circuit modeled by the given spice model and determine its function. Clearly determine the W/L ratio for the NMOS and PMOS transistors.

b. The plot generated by the given plot command is shown below. Determine which plot corresponds to v(2), v(3), and v(4). Justify your answer.

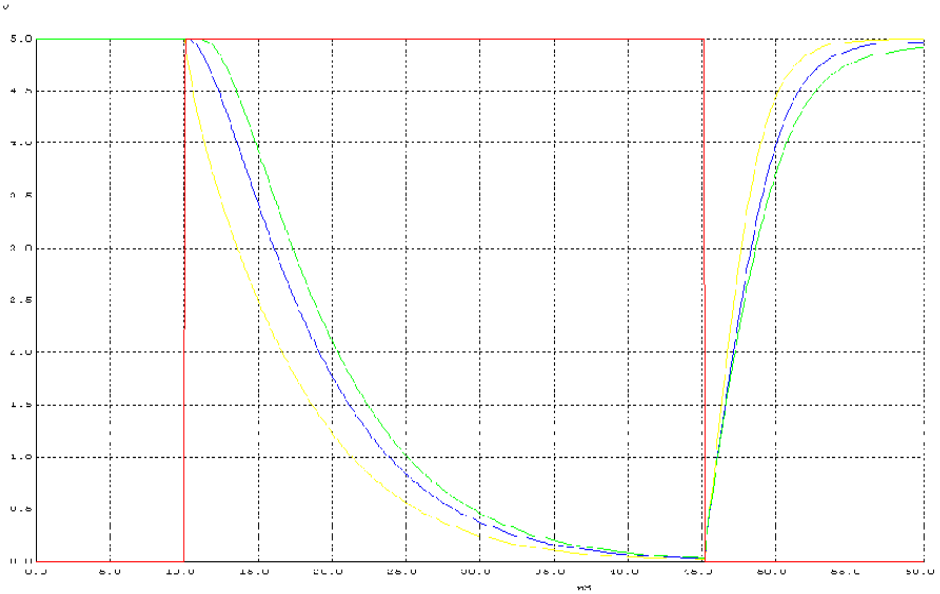


(2) Consider the spice model given below:

```
* Test Circuit2
.subckt g4 1 2 3 4 5 6 7
M1 4 1 0 0 nfet W=1u L=1u
M2 5 2 4 0 nfet W=1u L=1u
M3 6 3 5 0 nfet W=1u L=1u
M4 6 1 7 7 pfet W=2u L=1u
M5 6 2 7 7 pfet W=2u L=1u
M6 6 3 7 7 pfet W=2u L=1u
c1 4 0 0.2pf
c2 5 0 0.2pf
c3 6 0 0.5pf
.ends

x1 1 2 3 4   5  6 7  g4
x2 2 1 3 8   9 10 7  g4
x3 3 2 1 11 12 13 7 g4

Vdd 7 0 dc 5
V1 1 0 pulse(0 5 10ns 0ns 0ns 35ns 60ns)
V2 2 0 dc 5
V3 3 0 dc 5

.model nfet nmos (vto=1.0 KP=80u)
.model pfet pmos (vto=-1.0 KP=40u)

.tran 0.1ns 60ns
.plot tran v(1) v(6) v(10) v(13)
.end
```

a. Draw the transistor-level circuit modeled by the given spice model for **g4** and determine its function. Clearly determine the W/L ratio for the NMOS and PMOS transistors.

b. The plot generated by the given plot command is shown below. Determine which plot corresponds to v(6), v(10), and v(13). Justify your answer.

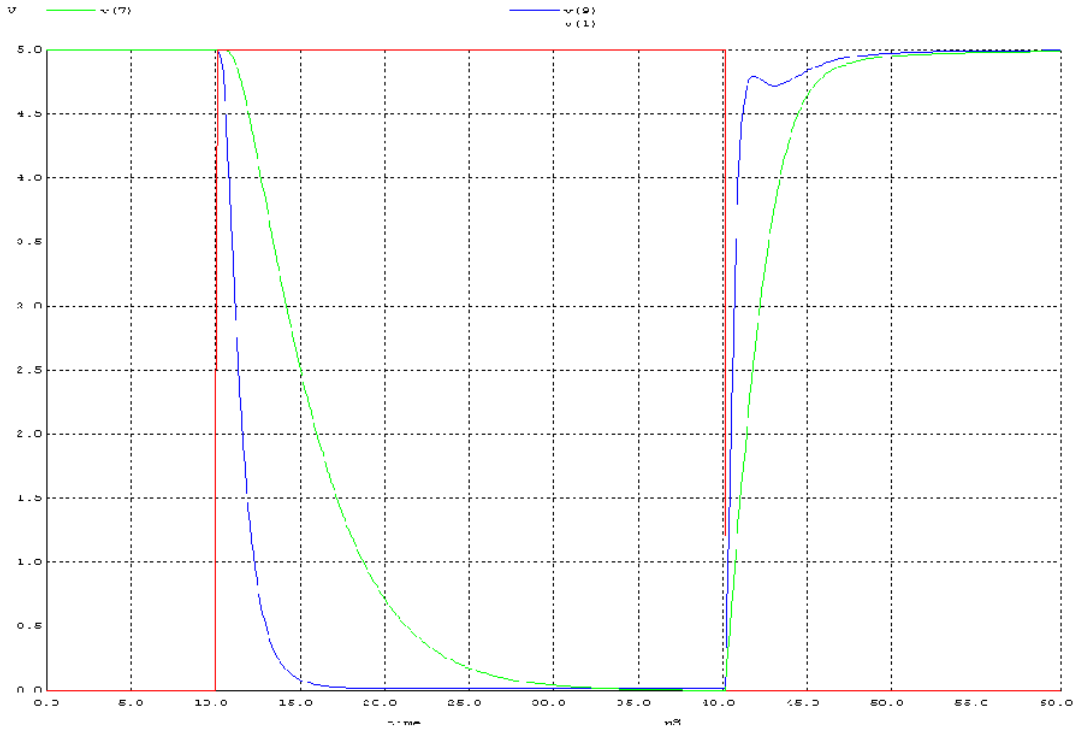


(3) Consider the spice model given below:

```
* Test Circuit3

M1 5 1 0 0 nfet W=1u L=1u
M2 6 2 5 0 nfet W=1u L=1u
M3 7 3 6 0 nfet W=1u L=1u
M4 7 1 10 10 pfet W=2u L=1u
M5 8 1 0 0 nfet W=1u L=1u
M6 9 7 8 0 nfet W=1u L=1u
M7 9 4 8 0 nfet W=1u L=1u
M8 9 1 10 10 pfet W=2u L=1u
c1 5 0 0.1pf
c2 6 0 0.1pf
c3 7 0 0.3pf
c4 8 0 0.1pf
c5 9 0 0.1pf

Vdd 10 0 dc 5
V1 1 0 pulse(0 5 10ns 0ns 0ns 30ns 60ns)
V2 2 0 dc 5
V3 3 0 dc 5
V4 4 0 dc 0


.model nfet nmos (vto=1.0 KP=80u)
.model pfet pmos (vto=-1.0 KP=40u)

.tran 0.1ns 60ns
.plot tran  v(1) v(7) v(9)
.end
```

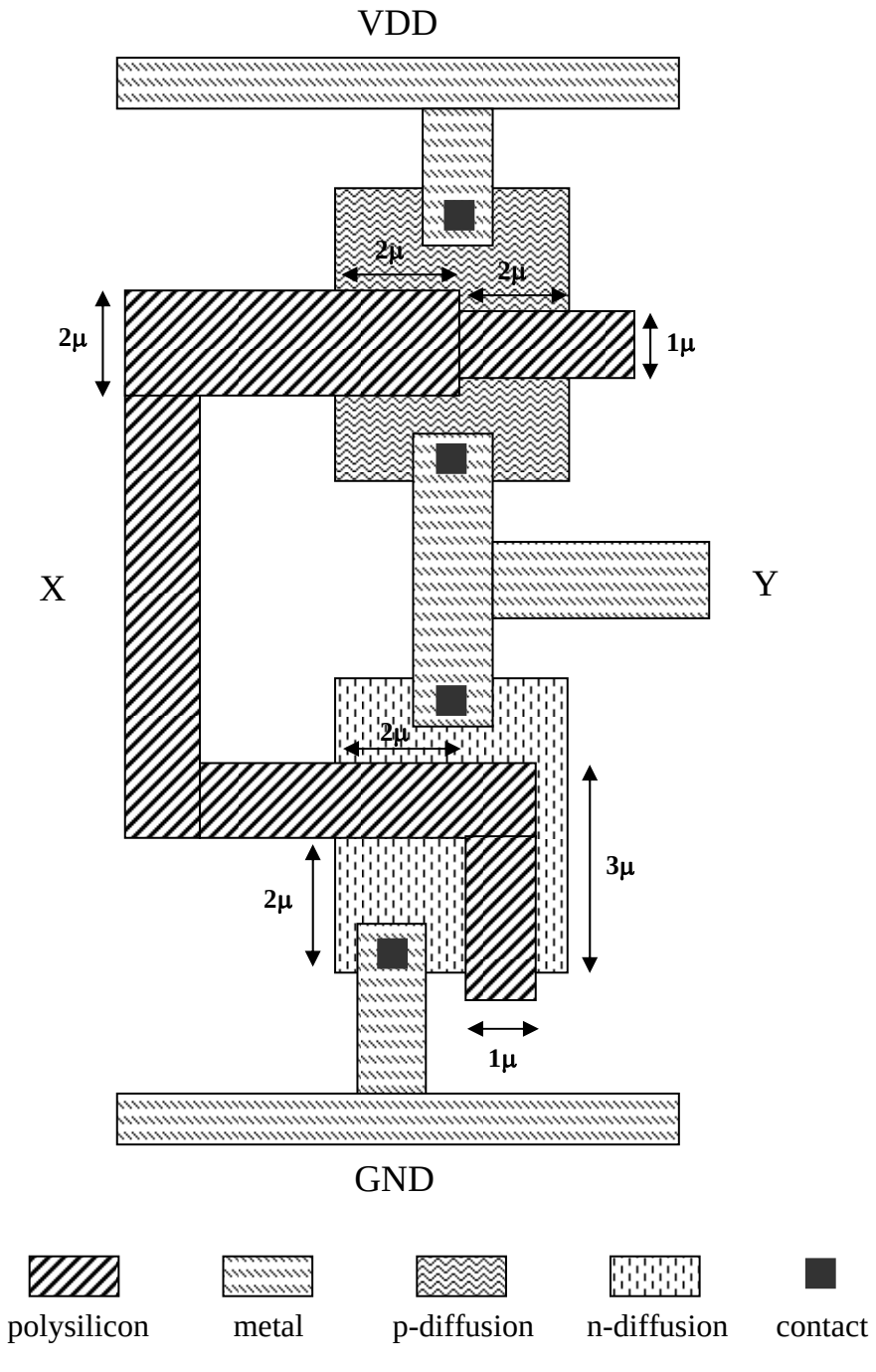
a. Draw the transistor-level circuit modeled by the given spice model and determine its function. Clearly determine the W/L ratio for the NMOS and PMOS transistors.

b. The plot generated by the given plot command is shown below. Is the plot for v(7) and v(9) the correct output that should be generated by the circuit. If the output is incorrect explain why and make necessary modifications in the circuit implementation to make the circuit produce correct output.



[10 Points]

(II) Given the layout shown below, determine the transistor-level circuit implemented by this layout. Calculate the channel resistance of the n- and p-transistors. Assume that the sheet resistance of the p-channel equals to $15X10^3$ *Ω/SQ*, and that of the n-channel equals to $6X10^3$ *Ω/SQ*. Assume that the value of the resistance of a corner square is equal to 0.66 the normal square resistance.

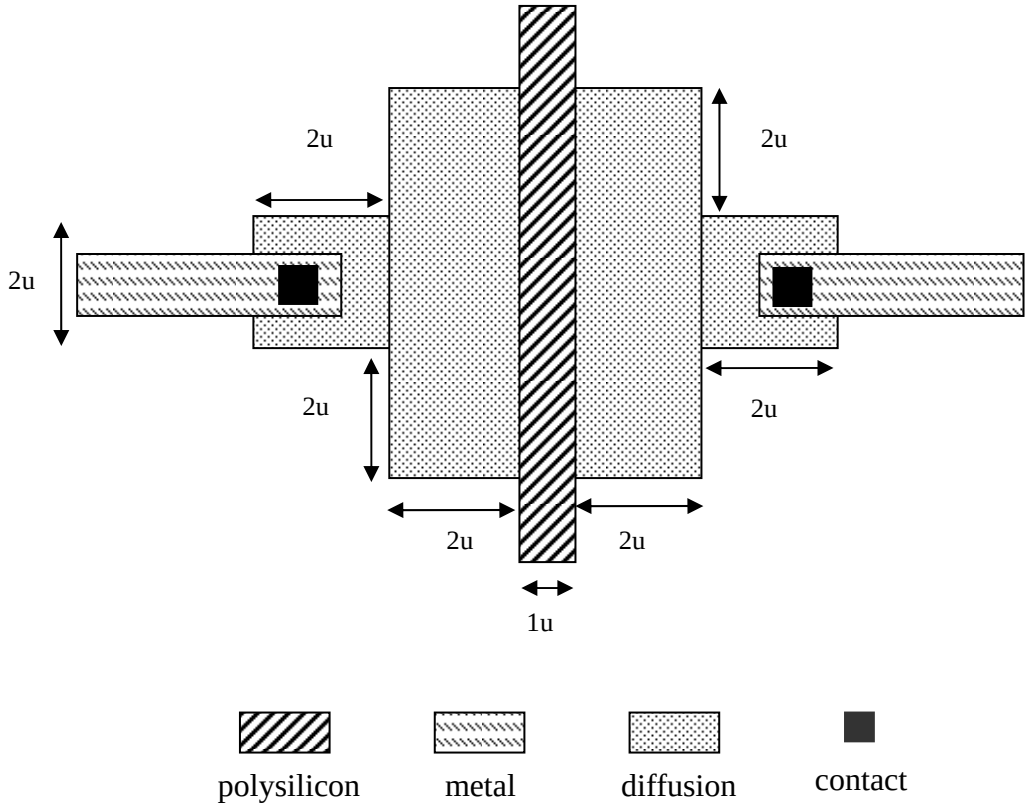


[20 points]

(III) Consider the CMOS inverter modeled in spice below:

```
Vdd   1   0   DC   5 VOLTS
M1      2  3  0  0          NFET   W=?  L=?  AS=?  AD=?  PS=?  PD=?
M2      2  3  1  1          PFET   W=?  L=?  AS=?  AD=?  PS=?  PD=?
.MODEL NFET   NMOS   VTO=1  GAMMA=0.4  KP=2.5E-5
+ TOX=200E-8
+CGBO=200P    CGSO=300P    CGDO=300P
+CJ=200U   CJSW=400P   MJ=0.5  MJSW=0.3   PB=0.7
.MODEL PFET   PMOS   VTO=-1  GAMMA=0.4  KP=1E-5
+ TOX=200E-8
+CGBO=200P    CGSO=300P    CGDO=300P
+CJ=200U   CJSW=400P   MJ=0.5  MJSW=0.3   PB=0.7
```

Assume that the layout of the NMOS and PMOS transistors is as shown below:



(1) Fill the fields shown in the model with a question mark i.e.

```
M1      2  3  0  0          NFET   W=?  L=?  AS=?  AD=?  PS=?  PD=?
M2      2  3  1  1          PFET   W=?  L=?  AS=?  AD=?  PS=?  PD=?
```

(2) Compute the **gate** and **drain capacitance** for the NMOS and PMOS transistors in the CMOS inverter. Assume that $\varepsilon\,\varepsilon_{sio2}=3.9X8.854X10^{-14}$ F/cm, and that drain capacitances are calculated when the output is 2.5 Volts. Note that the junction capacitance is described by $C_j=C_{j0}\,(1-(V_j/V_b))^{-m}$, where V_j is the junction voltage (negative for reverse bias), C_{j0} is the zero bias capacitance, and V_b is the built-in junction potential. Also note that the thickness of oxide, TOX, is given in *cm*, AS and AD are given in m^2, PS and PD are given in *m*, CGBO, CGSO, CGDO, and CJSW are

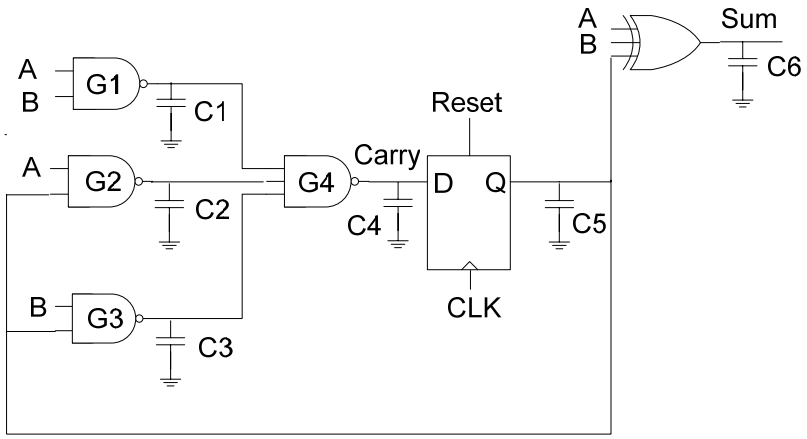
given in *F/m*, while CJ is given in F/m^2. (Note that it is important that you write the units correctly.)

(3) Assume that the CMOS inverter is driving **four** other equivalent CMOS inverters using a metal1 wire that is 1mm long, 1μm wide. Assume that metal1 capacitance is $30X10^{-18}$ F/μm^2, and its resistance is 4 *Ω/SQ*. Compute the **load capacitance** on the output of the driving inverter.

(4) Determine the **RC delay** from the inverter output across the metal1 wire. How wide should the metal1 wire be to make the delay for the inverter output across the wire less than or equal to 0.2 ns? Verify your answer.

[40 points]

(IV) Consider the **serial adder** design shown below. It is required to design the adder to operate at a **clock frequency** of **2 GHz** (i.e. **0.5ns cycle time**). Assume that the D-FF is rising-edge triggered and has the following parameters: **T_{setup}=75 pS, T_{hold}=25 pS, $T_{clk \rightarrow Q}$=125pS**. Assume that C4=100 fF, C5=200 fF, and C6=100 fF. Also, assume the the 3-input XOR gate has already been design and has a delay of 200 pS.



Assume that the circuit will be fabricated using a **1μ technolgy** CMOS process with the following parameters: **minimum grid size=0.1μ** , C_{ox}=2 fF/um^2, μ_n=400 cm^2/S.V, μ_p=200 cm^2/S.V, V_{tn}=0.8 V, V_{tp}=-0.8 V, and Vdd=5 V. Also, assume that for a CMOS inverter, t_{PLH} and t_{PHL} are given as 2.0 C_L/β_p (S) and 2.0 C_L/β_n (S), respectively. Note that $\beta=\mu * C_{ox} * W/L$

(1) **Design** the gates G1, G2, G3, and G4 using **static CMOS** (i.e. **determine the W/L ratios of the NMOS and PMOS transistors**) such that the serial adder works properly under the required **clock frequency of 2 GHz**. Assume that **t_{PLH}** and **t_{PHL}** are equivalent. Also assume that the delay across the gates G1, G2, G3, and G4 is equivalent. Furthermore, assume that the capactinaces C1, C2, and C3 are estimated based on the gate capacitance only.

(2) Show the transistor-level implementation of the Carry logic, i.e. G1, G2, G3, G4 using **2-stage DOMINO** logic using the smallest number of transistors possible. Do not assume the availability of inverted inputs. Does your implmentation suffer from Charge-Sharing problem? Suggest a solution for solving this problem.

(3) Show the transistor-level implementation of the Carry logic, i.e. G1, G2, G3, G4 using **2-stage NORA** logic using the smallest number of transistors possible. Do not assume the availability of inverted inputs.

(4) Determine the **dynamic power** dissipated by the serial adder for each of the following two clock cycles. Assume that the D-FF has an initial value of 0.