KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 360 Principles of VLSI Design
Term 071 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	S 8/9	No class.	
2	M 10/9	Syllabus. Introduction.	
3	W 12/9	VLSI system design process. Technology trends & logic complexity, Feature size and integration, Level of integration evolution, VLSI design flow, VLSI design example.	Chapter 1 (1.1, 1.3, 1.4, 1.5)
4	S 15/9	VLSI design example, Chip Manufacturing Process, Yield, Effect of Die Size on Yield. Mobility, Current density, Drift and Diffusion, Conductivity, Resistivity.	Chapter 1 (1.3) & Handout
5	M 17/9	Semiconductors, Silicon atom, Covalent Bonds, Concept of a hole, Conduction and Valence bands. Intrinsic semiconductors, Extrinsic Semiconductors.	Handout
6	W 19/9	Doners and Acceptors, n-type and p-type semiconductors. Mass Action Law, Charge neutrality law.	Handout
7	S 22/9	No Class.	
8	M 24/9 (ext.)	Fermi-level for n-type and p-type semiconductors, PN junction, depletion region. Forward-biased and reverse-biased PN junction. Junction breakdown, Transition capacitance.	Handout
9	W 26/9 (ext.)	NMOS and PMOS transistors structure. Basic specifications of digital circuits: V_{OH}, V_{OL}. (**Quiz#1**)	Handout
10	S 29/9 (ext.)	Basic specifications of digital circuits: V_{IH}, V_{IL}, NMH, NML, V_{th}, fanin and fanout, power dissipation, propagation delay. NMOS and PMOS as pass transistors. Transmission gate. NMOS, PMOS and CMOS inverter.	Handout
11	M 1/10 (ext.)	Implementation of logic gates in CMOS: NAND, NOR and general Boolean functions. Implementation of XOR, XNOR and 2x1 MUX using regular CMOS and transmission gates. Guidelines and	Handout

		examples for implementing general Boolean functions.	
12	W 3/10	No Class.	
13	S 20/10	Guidelines and examples for implementing general Boolean functions. SR Latch implementation, Implementation of D-Latch & D-FF based on transmission gate.	Handout
14	M 22/10	MOS transistor theory: accumulation, depletion and inversion modes, cutoff, saturation and linear regions. Voltage-Current equations of MOS transistor.	Handout, Chapter 3
15	W 24/10	Voltage-Current equations of MOS transistor. Channel Length Modulation, Effective Channel Length and Width. (**Quiz#2**)	Handout, Chapter 3
16	S 27/10	Energy Band Diagram for P-Type Substrate, Fermi potential, work function, Energy Band Diagrams for Components of MOS Structure, Flat band voltage, MOS Biased in Depletion Region, Depletion Region Charge, MOS Biased in Inversion Region.	Handout, Chapter 3
17	M 29/10	MOS & Depletion Capacitance, Threshold Voltage for MOS Transistor, Threshold Voltage Body Bias Effect.	Handout, Chapter 3
18	W 31/10	Threshold Voltage for PMOS Transistors, Threshold Voltage Example, Threshold Voltage Body Bias Example, Types of MOS transistors: Enhancement and Depletion. Summary of operation of MOS transistors.	Handout, Chapter 3
19	S 3/11	Measurement of Parameters (V_{T0}, γ, λ, k_n, k_p). Spice Tutorial.	Handout, Chapter 3
	U 4/11	MAJOR EXAM I	
20	M 5/11	Spice Tutorial.	Handout
21	W 7/11	Solution of Major Exam I.	
22	S 10/11	Spice Tutorial.	Handout
23	M 12/11	Spice Tutorial. CMOS Processing technology: Silicon gate process.	Handout, Chapter 2
24	W 14/11	Parasitic MOS transistor. Basic CMOS technology: Basic n-well CMOS process.	Handout, Chapter 2
25	S 17/11	Basic n-well CMOS process. Layout Design rules. Layout of CMOS Inverter.	Handout, Chapter 2
26	M 19/11	Layout of 2-input NAND & NOR gates. Layout design strategy of any function.	Handout, Chapter 7
27	W 21/11	Layout design of XOR gate using Transmission gate. Magic Tutorial.	Handout, Chapter 7

28	S 24/11	Magic Tutorial. **(Quiz#4)**	Handout
29	M 26/11	Magic Tutorial.	Handout
30	W 28/11	Resistive-load inverter: V_{OL}, V_{OH}, V_{IL}, V_{IH}**.**	Chapter 5
31	S 1/12	Resistive-load inverter: V_{th}, static power dissipation. Enhancement-Load Inverter: Saturated & Linear load inverters: V_{OH}, V_{OL}.	Chapter 5
32	M 3/12	Depletion-Load Inverter: V_{OL}, V_{OH}, V_{IL}, V_{IH}, power dissipation.	Chapter 5
33	W 5/12	CMOS inverter: V_{OL}, V_{OH}, V_{IL}, V_{IH}, $V_{th,}$ power dissipation.	Chapter 5
34	S 8/12	Inverter Equivalent Circuits. **(Quiz#6)**	Chapter 7
35	M 10/12	Delay time definitions, T_{PHL}, T_{PLH}, T_{rising}, $T_{falling}$. Calculation of delay times. CMOS inverter design under delay constraints.	Chapter 6
36	W 12/12	CMOS inverter design under delay constraints. Ring Oscillator Circuit.	Chapter 6
		HAJJ BREAK	
37	S 29/12	Resistance estimation. Capacitance Estimation: gate capacitance.	Handout, Chapter 3 & 7
38	M 31/12	Junction capacitance. Source and drain capacitances. Spice modeling of capacitances. Gate extrinsic capacitance. Inverter total Load Capacitance.	Handout, Chapter 3 & 6
	T 1/1	MAJOR EXAM II	
39	W 2/1	Load Capacitance of 2-input NAND and NOR gates. Interconnect capacitance. Elmore Delay Model. RC delay.	Handout, Chapter 6 & 7
40	S 5/1	**Solution of Major Exam II.**	
41	M 7/1	Dynamic power estimation. Node Switching Probability. Short Circuit Power.	Chapter 6
42	W 9/1	Power meter technique. Introduction to dynamic CMOS: Dynamic latch. Project Discussion.	Chapter 6, 9
43	S 12/1	Dynamic CMOS logic (precharge-evaluate), Domino Logic. Examples of Domino Logic.	Chapter 9
44	M 14/1	Charge sharing problem. Solutions to the charge-sharing problem.	Chapter 9
45	W 16/1	Manchester-Carry Chain Circuit. NORA logic. Examples of NORA logic. Zipper CMOS circuits	Chapter 9