Threshold Voltage

COE 360

Principles of VLSI Design

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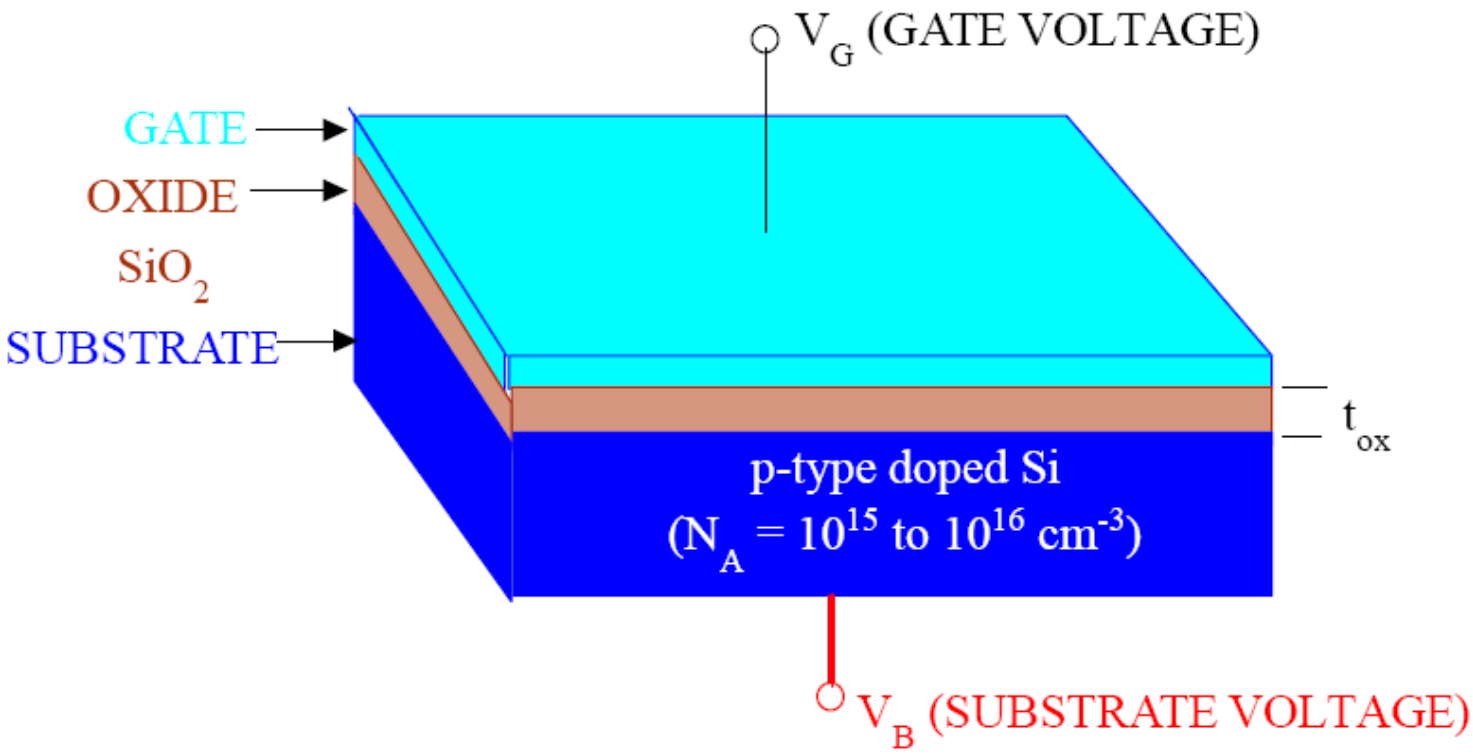
Outline

- Energy Band Diagrams for MOS Structure
- MOS in Equilibrium State
- MOS Biased in Depletion Region
- Depletion Region Charge
- MOS Biased in Inversion Region
- MOS & Depletion Capacitance
- Threshold Voltage for MOS Transistors
- Measurement of Parameters

Based on Slides of Kenneth R. Laker, University of Pennsylvania

TWO TERMINAL MOS STRUCTURE



EQUILIBRIUM: $n\,p = n_i^2$ ($n_i \approx 1.45 \times 10^{10}$ cm^{-3})

(BULK concentrations) $n_{p0} \approx \dfrac{n_i^2}{N_A}$ and $p_{p0} = N_A$

Energy Band Diagram for P-Type Substrate

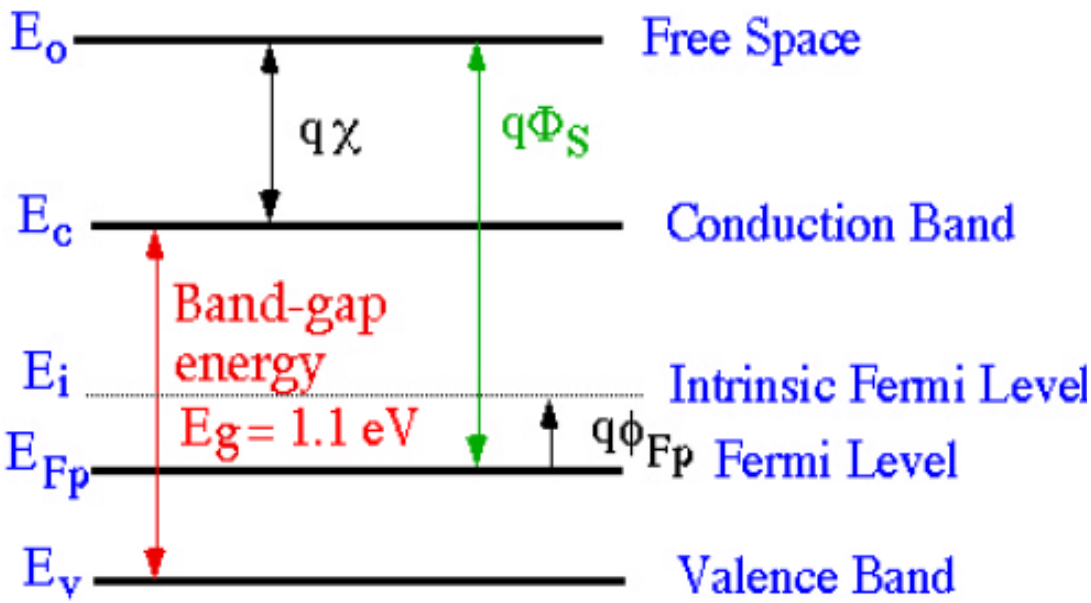
- The Fermi potential ϕ_F denotes the difference between the intrinsic Fermi level E_i and the Fermi level E_F

$$\phi_F = \frac{E_F - E_i}{q} \qquad \phi_{Fp} = \frac{kT}{q}\ln\frac{n_i}{N_A} \quad (N_A >> n_i) \qquad \phi_{Fn} = \frac{kT}{q}\ln\frac{N_D}{n_i} \quad (N_D >> n_i)$$

- The electron affinity of silicon, $q\chi$, is the potential difference between the conduction level and vacuum (free space)
- The energy required for an electron to move from Fermi level into free space is called the work function $q\Phi_S$

$$q\Phi_S = q\chi + (E_c - E_F)$$

Energy Band Diagram for P-Type Substrate



qX = electron affinity of Si

$$\phi_F = \frac{E_F - E_i}{q}$$

Work Function

$$q\Phi_S = q\chi + (E_c - E_F)$$

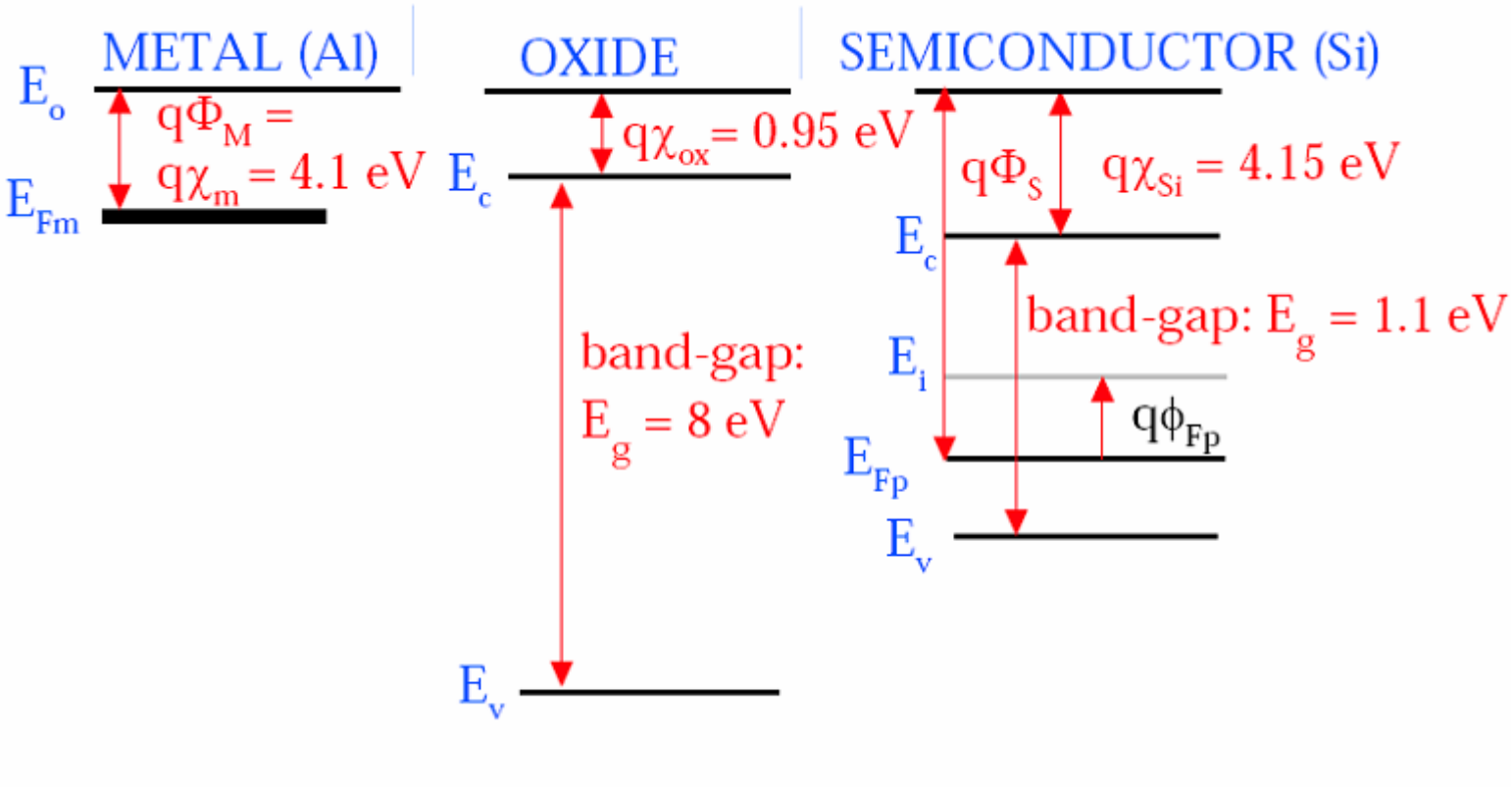
$$\phi_{Fn} = \frac{kT}{q} \ln \frac{N_D}{n_i} \quad (N_D >> n_i)$$

$$\phi_{Fp} = \frac{kT}{q} \ln \frac{n_i}{N_A} \quad (N_A >> n_i)$$

$n_i = 1.45 \times 10^{10}$ cm^{-3} @ room temp,
$k = 1.38 \times 10^{-23}$ J/°K,
$q = 1.6 \times 10^{-19}$ C

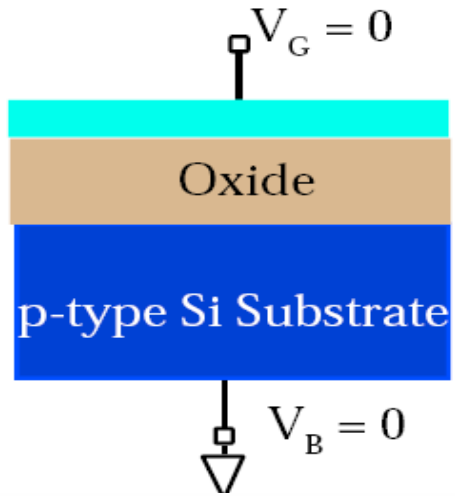
=> $kT/q = 26$ mV @ room temp

Energy Band Diagrams for Components of MOS Structure



MOS in Equilibrium State

Under Thermal Equilibrium:
Fermi level of all materials
Must line up.

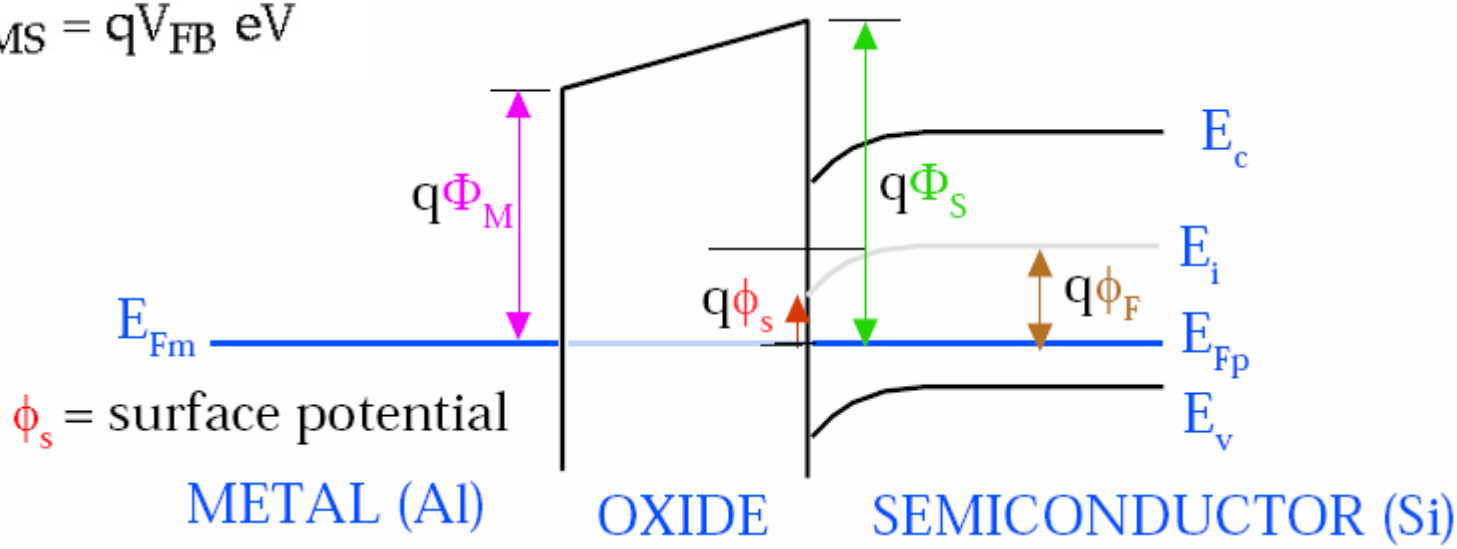


Flat-band voltage:

$V_{FB} = \Phi_M - \Phi_S$ volts

Built-in potential:

$\Phi_{MS} = qV_{FB}$ eV



Flat Band Voltage

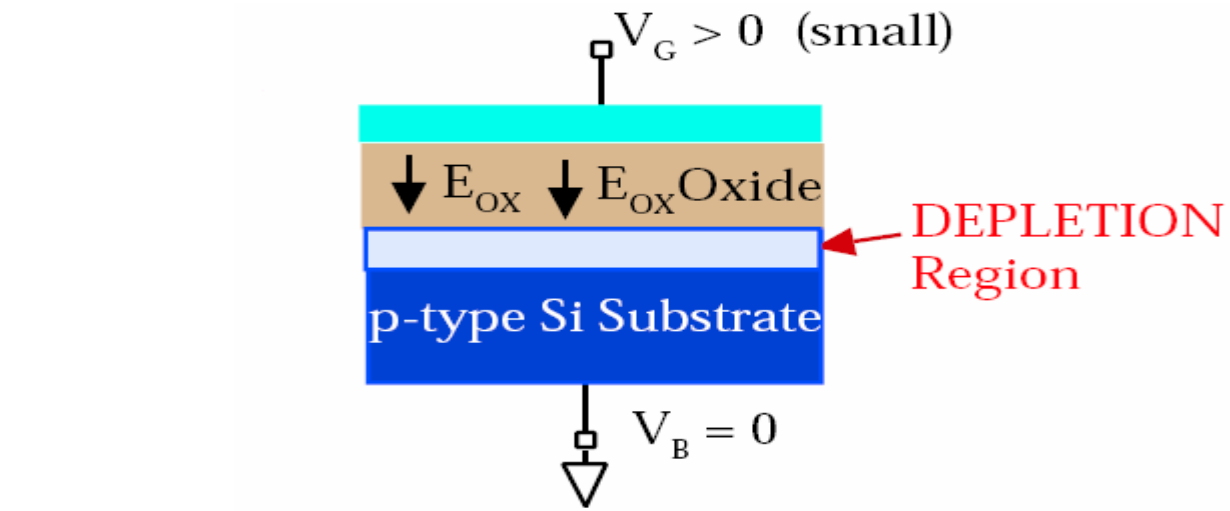
- Consider a MOS structure of p-type silicon substrate, a silicon dioxide layer and aluminum gate
- Equilibrium Fermi Potential of silicon is $q\phi_{Fp} = 0.2$ eV
- The work function $q\Phi_S = 4.15$ eV + 1.1/2 eV + 0.2 eV

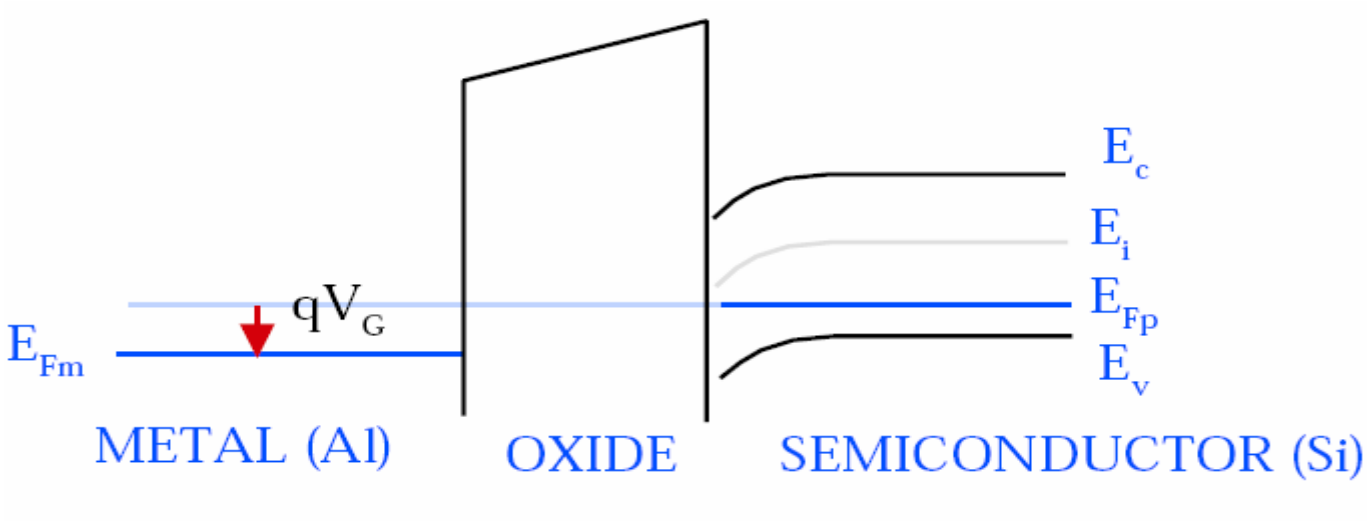
  $= 4.15$ eV + 0.75 eV = 4.9 eV
- The built-in potential difference across this MOS systems is $q\Phi_M - q\Phi_S = 4.1$ eV – 4.9 eV = -0.8 eV
- If a voltage corresponding to this potential difference is applied between gate and substrate the energy bands become flat.

Flat-band voltage:

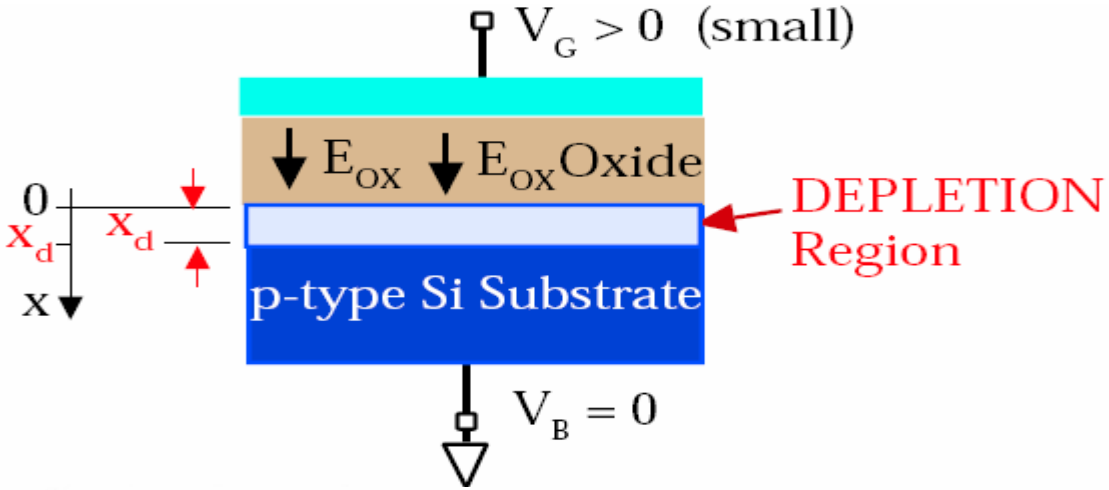
$V_{FB} = \Phi_M - \Phi_S$ volts

MOS Biased in Depletion Region





Depletion Region Charge



$$dQ = -qN_A dx$$

Mobile charge in thin layer parallel to Si surface

$$d\phi = -\frac{x}{\varepsilon_{Si}} dQ = x\frac{qN_A}{\varepsilon_{Si}} dx$$

Change in surface potential to displace dQ

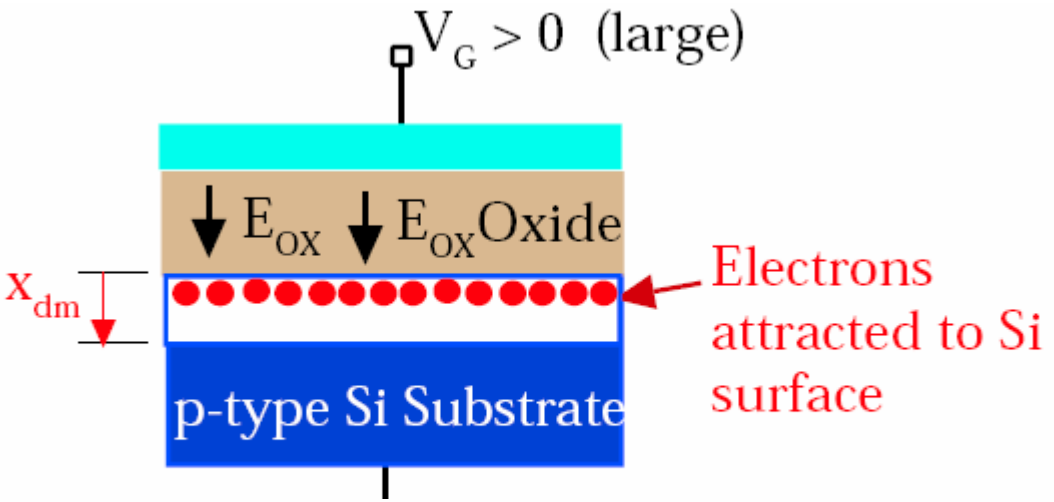
$$\int_{\phi_s}^{\phi_F} d\phi = \int_0^{x_d} x\frac{qN_A}{\varepsilon_{Si}} dx \rightarrow \phi_F - \phi_s = \frac{qN_A}{2\varepsilon_{Si}} x_d^2$$

$$x_d = \sqrt{\frac{2\varepsilon_{Si}|\phi_F - \phi_s|}{qN_A}}$$

Depletion Region Charge

$$Q = -qN_A x_d = -\sqrt{2qN_A\varepsilon_{Si}|\phi_F - \phi_s|}$$

MOS Biased in Inversion Region

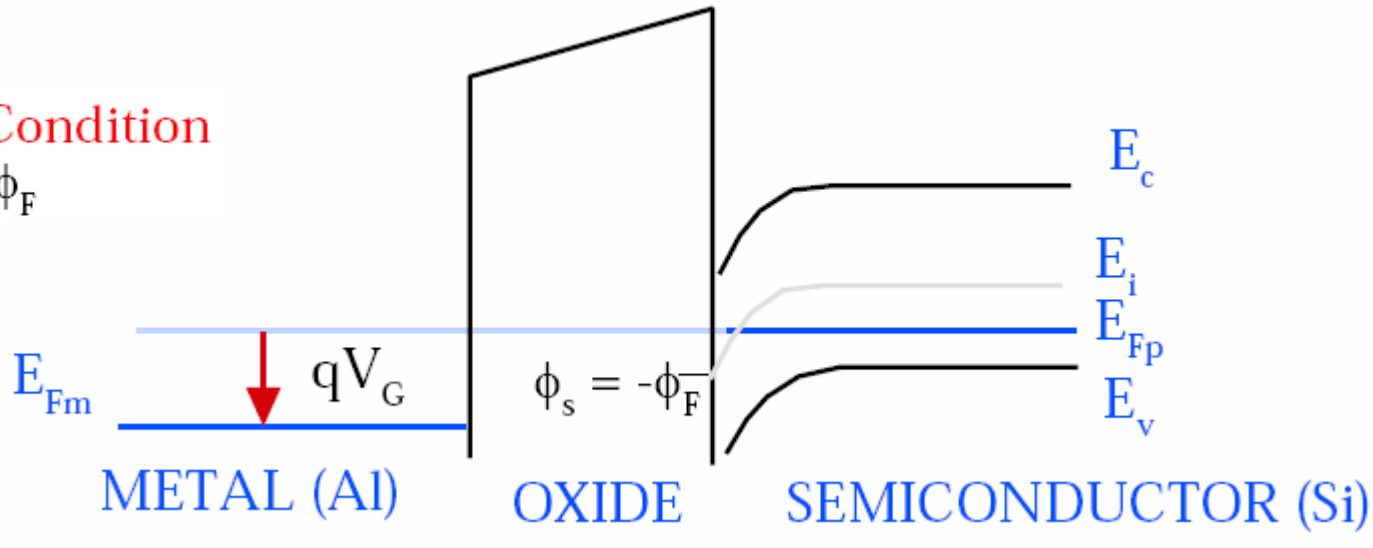


$$x_{dm} = x_d\Big|_{\phi_s=-\phi_F} = \sqrt{\frac{2\varepsilon_{Si}\,|2\phi_F|}{qN_A}}$$

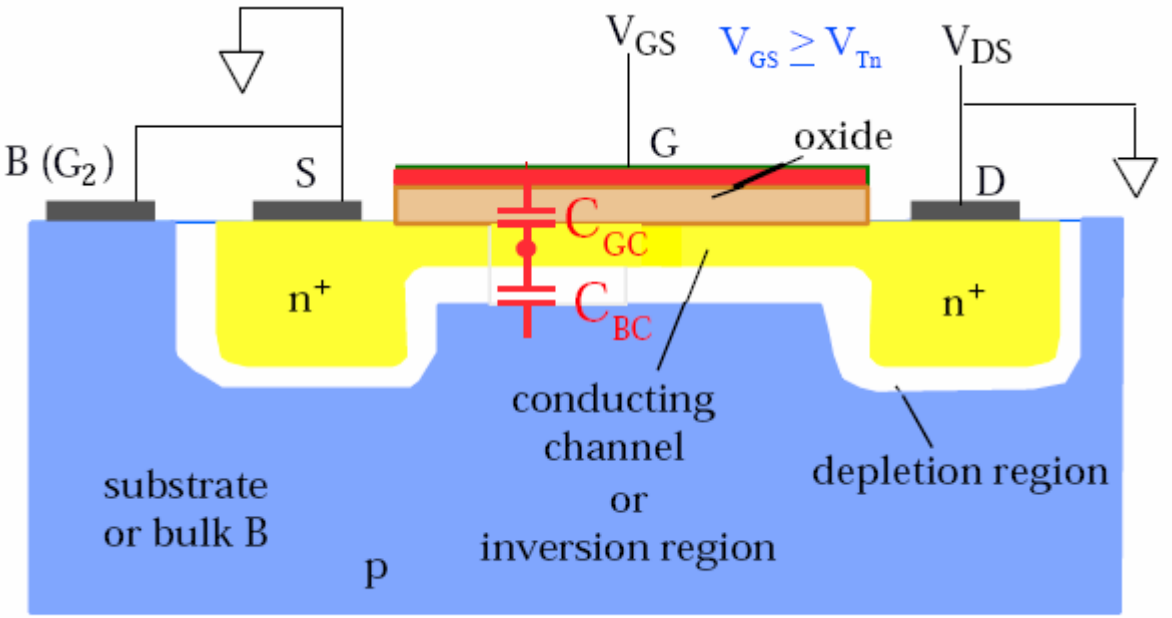
$$Q_{B0} = Q\Big|_{x_{dm}=x_d} - qN_A x_{dm} = -\sqrt{2qN_A\varepsilon_{Si}|2\phi_F|}$$

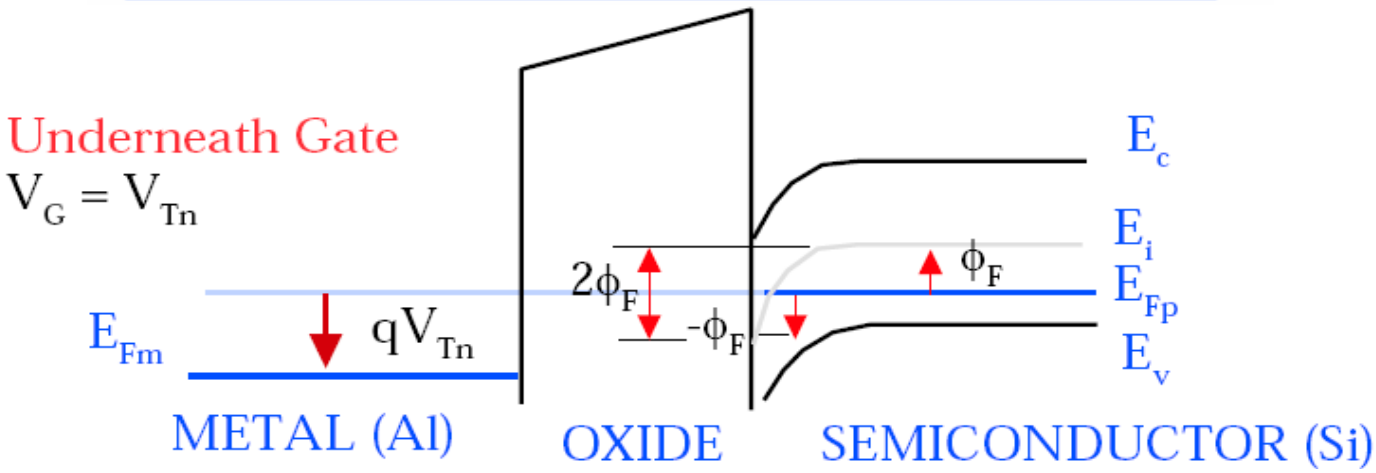
Inversion Condition

$\phi_s = -\phi_F$



MOS Biased in Inversion Region





MOS & Depletion Capacitance

MOS Capacitance $C_{GC} = WLC_{ox}$, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ [t_{ox} -> TOX in SPICE] [C_{ox} -> COX in SPICE]

$t_{ox} = 50$ nm, $\varepsilon_{ox} = 0.34$ pF/cm => $C_{ox} = 6.8 \times 10^{-8}$ F/cm^2

Depletion Capacitance $C_{BC} = WLC_j$, $C_j = \frac{\varepsilon_{Si}}{x_d}$

$$x_d = \sqrt{\frac{2\varepsilon_{Si}|\phi_F - V_{SB}|}{qN_A}}$$

[N_{SUB} -> NSUB in SPICE]

N_{SUB} (p - substrate)

$$\phi_{Fp} = \frac{kT}{q} \ln \frac{n_i}{N_A}$$

$N_A = 3 \times 10^{17}$ cm^{-3}, $n_i = 1.45 \times 10^{10}$ cm^{-3} => $\phi_F = -0.438$ V

(recall that at room temp or 27°C kT/q = 26 mV)

$V_{SB} = 0$ V, $\varepsilon_{Si} = 1.06$ pF/cm, $q = 1.6 \times 10^{-19}$ C, N_A, ϕ_F => $x_d = 6.22$ μm

ε_{Si}, x_d => $C_j = 0.17 \times 10^{-8}$ F/cm^2

W x L = 50 μm x 50 μm => $C_{BC} = 42.5$ fF

Threshold Voltage for MOS Transistor

- Components of Threshold Voltage:
  - Work function difference between gate and channel
  - Gate voltage component to change surface potential
  - Gate voltage component to offset depletion region charge
  - Voltage component to offset fixed charges in gate oxide and silicon oxide interface
- Threshold voltage is:

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

Threshold Voltage for MOS Transistors

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

(+ for nMOS and - for pMOS)

$\Phi_{GC} = \phi_F(\text{substrate}) - \phi_M$ metal gate

$\Phi_{GC} = \phi_F(\text{substrate}) - \phi_F(\text{gate})$ polysilicon gate

$$Q_{B0} = -\sqrt{2qN_A\varepsilon_{Si}|2\phi_F|}$$

[$2\phi_F$ = PHI in SPICE]

[N_A = NSUB in SPICE]

For $V_{SB} = 0$, the threshold voltage is denoted as

V_{T0} or $V_{T0n,p}$ [V_{T0} -> VT0 in SPICE]

[Q_{ox} = qNSS in SPICE]

Threshold Voltage factors:

-> Gate conductor material;

-> Gate oxide material & thickness;

-> Channel doping;

-> Impurities in Si-oxide interface;

-> Source-bulk voltage V_{sb};

-> Temperature.

Threshold Voltage for MOS Transistors

For $V_{SB} \neq 0$: the threshold voltage is denoted as V_T or $V_{Tn,p}$

$$Q_B = -\sqrt{2qN_A\varepsilon_{Si}|2\phi_F - V_{SB}|}$$

$$V_T = \Phi_{GC} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$$= \underbrace{\Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}}_{V_{T0}} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

where

$$\frac{Q_B - Q_{B0}}{C_{ox}} = \underbrace{\sqrt{\frac{2qN_A\varepsilon_{Si}}{C_{ox}}}}_{\gamma}\left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

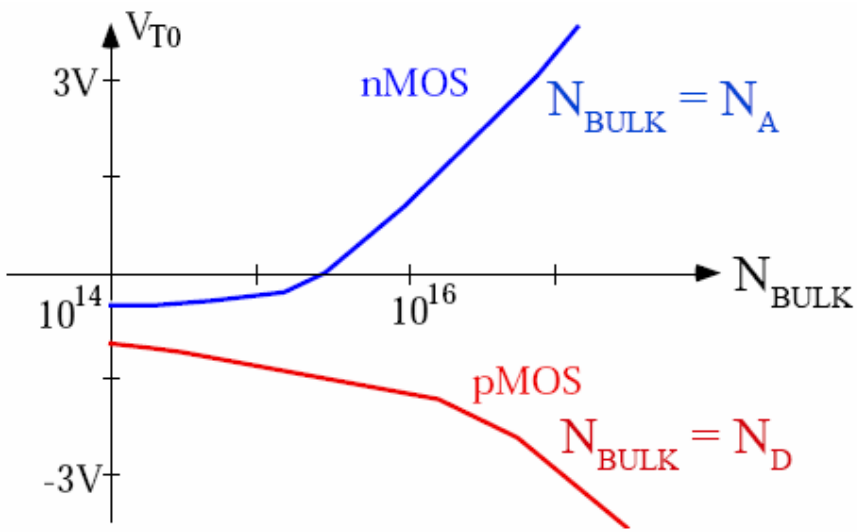
(γ = Body-effect coefficient) [γ = GAMMA in SPICE]

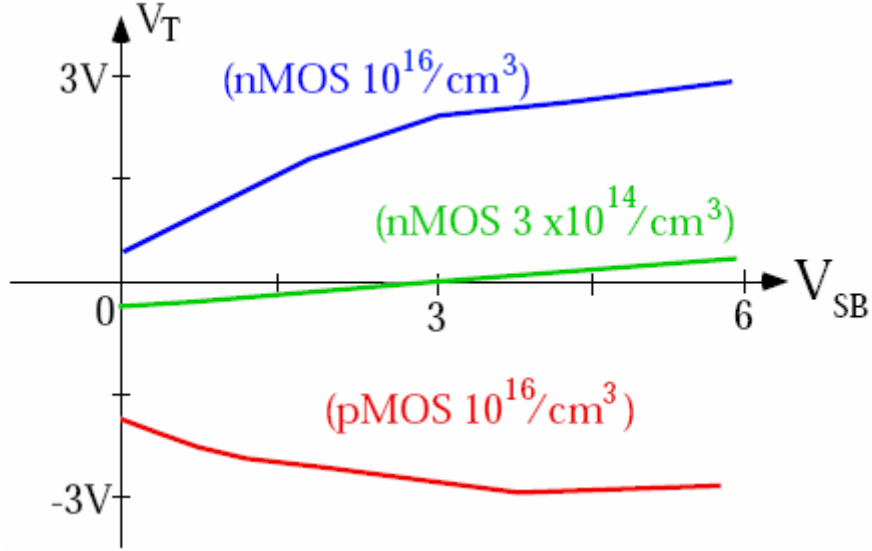
$$V_{Tn} = V_{T0n} + \gamma\left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

Threshold Voltage for MOS Transistors

n-channel -> p-channel

- ϕ_F is negative in nMOS, positive in pMOS
- Q_{B0}, Q_B are negtive in nMOS, positive in pMOS
- γ is positive in nMOS, negative in pMOS
- V_{SB} is positive in nMOS, negative in pMOS





Threshold Voltage Example

EXAMPLE Calculate the threshold voltage V_{T0} at $V_{BS} = 0$, for a polysilicon gate n-channel MOS transistor with the following parameters:

substrate doping density $N_A = 10^{16}$ cm^{-3},
polysilicon doping density $N_D = 2 \times 10^{20}$ cm^{-3},
gate oxide thickness $t_{ox} = 500$ Angstroms,
oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}.

$$V_{T0} = \Phi_{GC} - 2\phi_{F(sub)} - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

$\phi_{F(sub)}$, Φ_{GC}: $\Phi_{GC} = \phi_{F(sub)} - \phi_{F(gate)}$

$$\phi_{F(sub)} = \frac{kT}{q} \ln \frac{n_i}{N_A} = 0.026\text{V} \ln\left(\frac{1.45 \times 10^{10}}{10^{16}}\right) = -0.35\text{V}$$

$$\phi_{F(gate)} = \frac{kT}{q} \ln \frac{N_D}{n_i} = 0.026\,\text{V} \ln\left(\frac{2 \times 10^{20}}{1.45 \times 10^{10}}\right) = 0.60\,\text{V}$$

$$\Phi_{GC} = \phi_{F(sub)} - \phi_{F(gate)} = \text{-0.35 V - 0.60 V = -0.95 V}$$

Threshold Voltage Example

$$V_{T0} = \Phi_{GC} - 2\phi_{F(sub)} - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

Q_{B0}:

$$Q_{B0} = -\sqrt{2qN_A\varepsilon_{Si}|2\phi_{F(sub)}|}$$

$$= -\sqrt{2(1.6\text{x}10^{-19}\,\text{C})(10^{16}\,\text{cm}^{-3})(1.06\text{x}10^{-12}\,\text{Fcm}^{-1})\,|2\text{x}0.35\text{V}|}$$

F = C/V

$$= -4.87 \text{ x } 10^{-8}\,\text{C/cm}^2$$

C_{ox}:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{0.34\text{x}10^{-12}\,\text{Fcm}^{-1}}{500\text{x}10^{-8}\,\text{cm}} = 6.8\text{x}10^{8}\,\text{F/cm}^2$$

Q_{ox}:

$$Q_{ox} = qN_{ox} = (1.6\text{x}10^{-19}\,\text{C})(4\text{x}10^{10}\,\text{cm}^{-2}) = 6.4\text{x}10^{-9}\,\text{C/cm}^2$$

$$\frac{Q_{B0}}{C_{ox}} = \frac{-4.87\text{x}10^{8}\,\text{C/cm}^2}{6.8\text{x}10^{8}\,\text{F/cm}^2} = -0.716\,\text{V} \qquad \frac{Q_{ox}}{C_{ox}} = \frac{6.4\text{x}10^{-9}\,\text{C/cm}^2}{6.8\text{x}10^{8}\,\text{F/cm}^2} = 0.094\,\text{V}$$

$$V_{T0} = -0.95\text{V} - (-0.70\,\text{V}) - (-0.72\,\text{V}) - (0.09\text{V}) = 0.38\text{V}$$

Threshold Voltage Body Bias Example

EXAMPLE Consider the n-channel MOS transistor with the following process parameters:

substrate doping density $N_A = 10^{16}\ cm^{-3}$,
polysilicon doping density $N_D = 2 \times 10^{20}\ cm^{-3}$,
gate oxide thickness $t_{ox} = 500$ Angstroms,
oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}\ cm^{-2}$.

In digital circuit design, the condition $V_{SB} = 0$ can not always be quaranteed for all transistors. Plot the threshold voltage V_T as a function of V_{SB}.

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

γ - Body-effect coefficient:

F = C/V

$$\gamma = \frac{\sqrt{2qN_A e_{Si}}}{C_{ox}} = \frac{\sqrt{2(1.6\times10^{-19}\,C)(10^{16}\,cm^{-3})(1.06\times10^{-12}\,F/cm)}}{6.8\times10^{-8}\,F/cm^2}$$

$$= \frac{5.824\times10^{-8}\,C/V^{1/2}cm^2}{6.8\times10^{-8}\,C/Vcm^2} = 0.85\,V^{1/2}$$

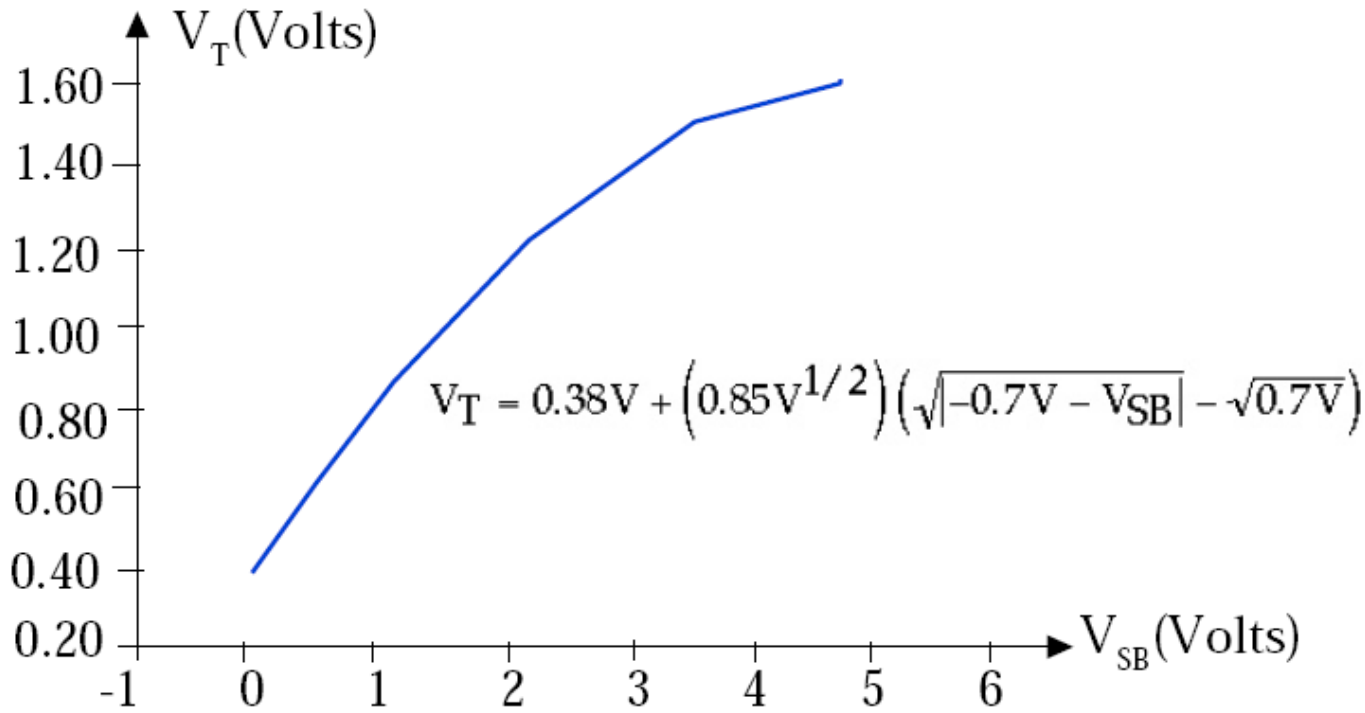
Threshold Voltage Body Bias Example

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

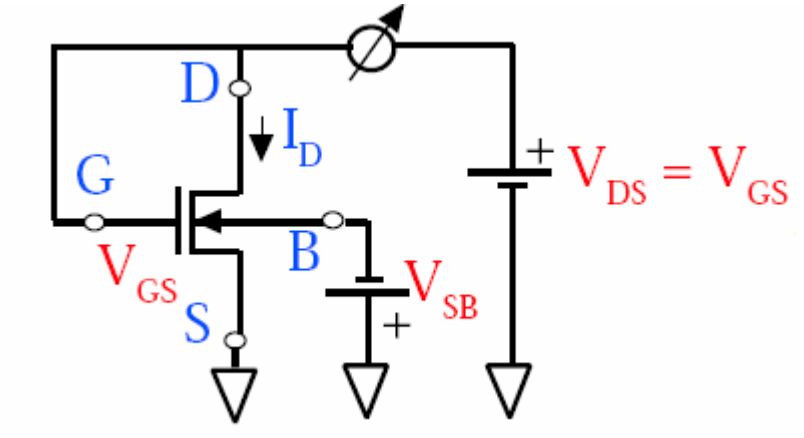
where

$$V_{T0} = 0.38V$$

$$\gamma = 0.85V^{1/2}$$



Measurement of Parameters (V_{T0}, γ, λ, k_n, k_p)



$$k_n = \mu_n C_{ox} \frac{W}{L} \qquad k_p = \mu_p C_{ox} \frac{W}{L}$$

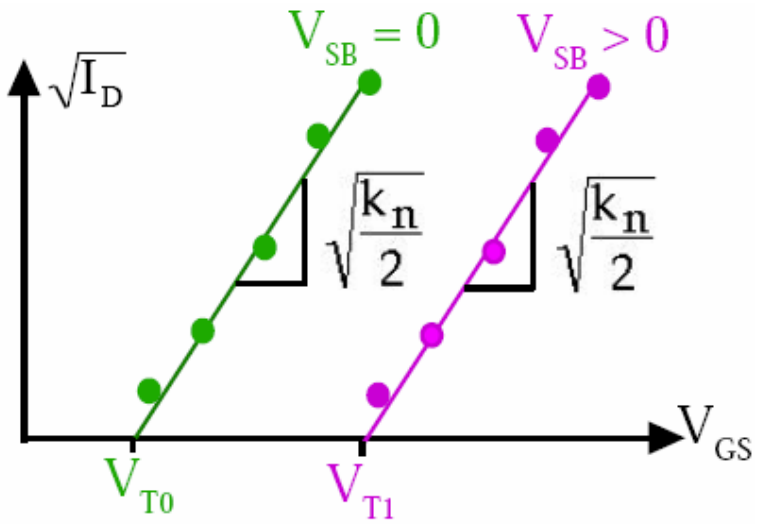
$$I_D(sat) = \frac{k_n}{2}(V_{GS} - V_{T0})^2$$

$$\sqrt{I_D(sat)} = \sqrt{\frac{k_n}{2}}(V_{GS} - V_{T0})$$

Gamma

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

$$\gamma = \frac{V_T(V_{SB}) - V_{T0}}{\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|}}$$



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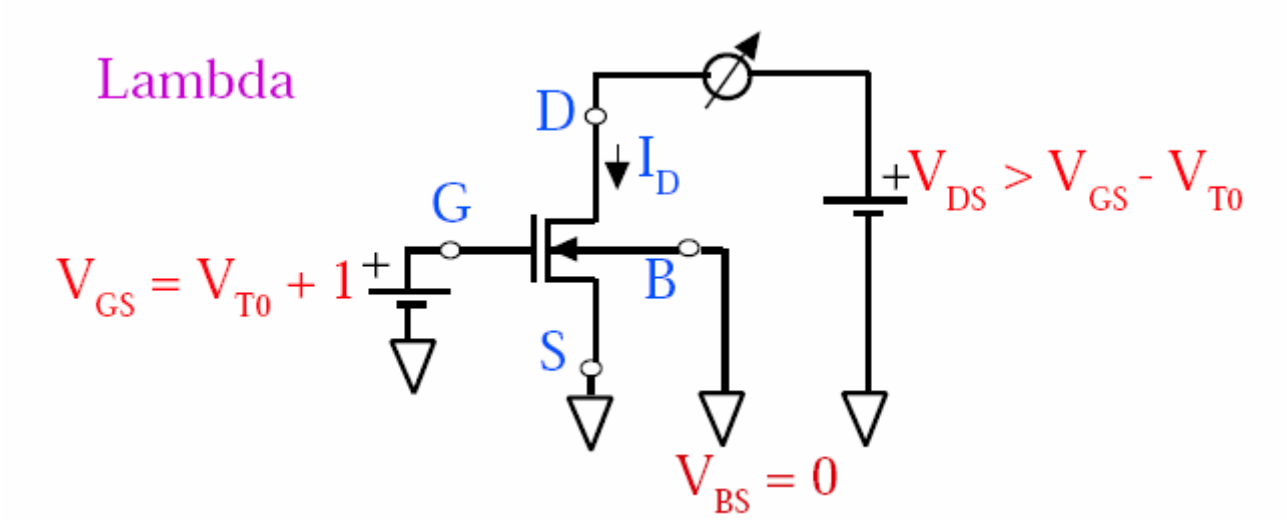

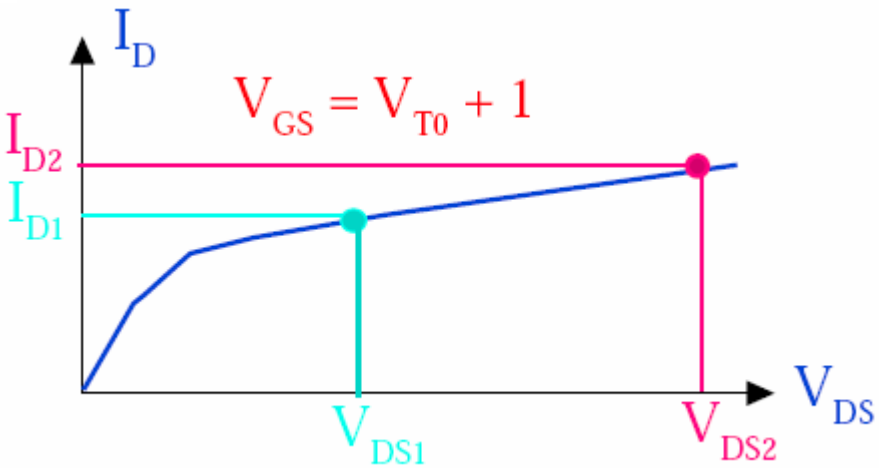

$$I_D(sat) = k_n(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})$$

$$V_{GS} = V_{T0} + 1$$

$$\frac{I_{D2}}{I_{D1}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$