COE 360 Principles of VLSI Design
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CMOS Design Under Delay Constraints
Example

EXAMPLE 6.3

A company has access to a CMOS fabrication process with the device parameters listed below.

$\mu_n C_{ox} = 120\,\mu\text{A/V}^2$
$\mu_p C_{ox} = 60\,\mu\text{A/V}^2$
$L = 0.6\,\mu\text{m}$ for both nMOS and pMOS devices
$V_{T0,n} = 0.8\text{ V}$
$V_{T0,p} = -1.0\text{ V}$
$W_{min} = 1.2\,\mu\text{m}$

Design a CMOS inverter by determining the channel widths W_n and W_p of the nMOS and pMOS transistors, to meet the following performance specifications.

- $V_{th} = 1.5\text{ V}$ for $V_{DD} = 3\text{ V}$,
- Propagation delay times $\tau^*_{PHL} \leq 0.2$ ns and $\tau^*_{PLH} \leq 0.15$ ns,
- A falling delay of 0.35 ns for an output transition from 2 V to 0.5 V, assuming a combined output load capacitance of 300 fF and ideal step input.

We start our design by satisfying the time delay constraints. First, the *minimum* (W/L) ratios of the nMOS and pMOS transistors which are dictated by the propagation delay constraints can be found using (6.33) and (6.34), as follows.

$$\left(\frac{W_n}{L_n}\right) = \frac{C_{load}}{\tau^*_{PHL}\mu_n C_{ox}(V_{DD} - V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right]$$

$$= \frac{300 \times 10^{-15}}{0.2 \times 10^{-9} \cdot 120 \times 10^{-6} \cdot (3 - 0.8)}\left[\frac{2 \cdot 0.8}{3 - 0.8} + \ln\left(\frac{4(3 - 0.8)}{3} - 1\right)\right]$$

$$= 7.9$$

$$\left(\frac{W_p}{L_p}\right) = \frac{C_{load}}{\tau^*_{PLH}\mu_p C_{ox}(V_{DD} - |V_{T,p}|)}$$

$$\times\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1\right)\right]$$

$$= \frac{300 \times 10^{-15}}{0.15 \times 10^{-9} \cdot 60 \times 10^{-6} \cdot (3 - 1)}\left[\frac{2 \cdot 1}{3 - 1} + \ln\left(\frac{4(3 - 1)}{3} - 1\right)\right]$$

$$= 25.2$$

During the falling output transition (from 2 V to 0.5 V), the nMOS transistor of the CMOS inverter will operate entirely in the linear region. The current equation of the nMOS transistor in this region is

$$C_{load}\frac{dV_{out}}{dt} = -\frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}\left[2(V_{OH} - V_{T0,n})V_{out} - V_{out}^2\right]$$

By integrating this expression, we obtain the following relationship.

$$t_{delay} = 0.35 \times 10^{-9} = -2C_{load} \int_{V_{out}=2}^{V_{out}=0.5} \frac{dV_{out}}{\mu_n C_{ox} \frac{W_n}{L_n} [2(V_{OH} - V_{T0,n})V_{out} - V_{out}^2]}$$

$$t_{delay} = \frac{-C_{load}}{\mu_n C_{ox} \frac{W_n}{L_n}} \frac{1}{(V_{OH} - V_{T0,n})} \ln \left(\frac{V_{out}}{2(V_{OH} - V_{T0,n}) - V_{out}} \right) \Bigg|_2^{0.5}$$

$$t_{delay} = \frac{-C_{load}}{\mu_n C_{ox} \left(\frac{W_n}{L_n} \right)} \frac{1}{(3 - 0.8)} \left[\ln \left(\frac{0.5}{2(3 - 0.8) - 0.5} \right) - \ln \left(\frac{2}{2(3 - 0.8) - 2} \right) \right]$$

$$0.35 \times 10^{-9} = \frac{-300 \times 10^{-15}}{120 \times 10^{-6} \left(\frac{W_n}{L_n} \right) 2.2} [-2.054 + 0.182]$$

Now we solve this equation for the nMOS transistor (W/L) ratio:

$$\left(\frac{W_n}{L_n} \right) = 6.1$$

Notice that this ratio is *smaller* than the (W/L)-ratio found from the propagation delay constraint. Thus, we take the larger ratio which will satisfy both timing constraints, and determine the size of the nMOS transistor as $W_n = 4.7\,\mu$m, for the given $L_n = 0.6\,\mu$m. Next, the logic threshold constraint of $V_{th} = 1.5$ V will help determine the pMOS transistor dimensions. Using (5.87) for the logic threshold voltage of the CMOS inverter,

$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}}(V_{DD} + V_{T0,p})}{1 + \sqrt{\frac{1}{k_R}}} = 1.5$$

we find that the ratio k_R which satisfies this design constraint is equal to 0.51. This value can now be used to calculate the (W/L)-ratio of the pMOS transistor, as follows.

$$k_R = \frac{\mu_n C_{ox} \left(\frac{W_n}{L_n} \right)}{\mu_p C_{ox} \left(\frac{W_p}{L_p} \right)} = \frac{120 \times 10^{-6}\,(7.9)}{60 \times 10^{-6} \left(\frac{W_p}{L_p} \right)} = 0.51$$

$$\left(\frac{W_p}{L_p} \right) = 31$$

Note that this ratio is *larger* than the one found from the propagation delay constraint earlier. Since the larger ratio will satisfy both the timing constraint and the V_{th}-constraint, we determine the pMOS transistor size as $W_p = 18.6\,\mu$m, for the given $L_p = 0.6\,\mu$m.