

William Stallings Data and Computer Communications

Chapter 6 The Data Communications Interface

Asynchronous and Synchronous Transmission

- ⌘ Typically, data transmitted serially over transmission medium.
- ⌘ For receiver to sample incoming bits properly, it must know
 - ☒ Arrival time
 - ☒ Duration of each bit
- ⌘ To receive bits correctly, timing of transmitter and receiver needs to be synchronized.
- ⌘ Two solutions for synchronization
 - ☒ Asynchronous
 - ☒ Synchronous

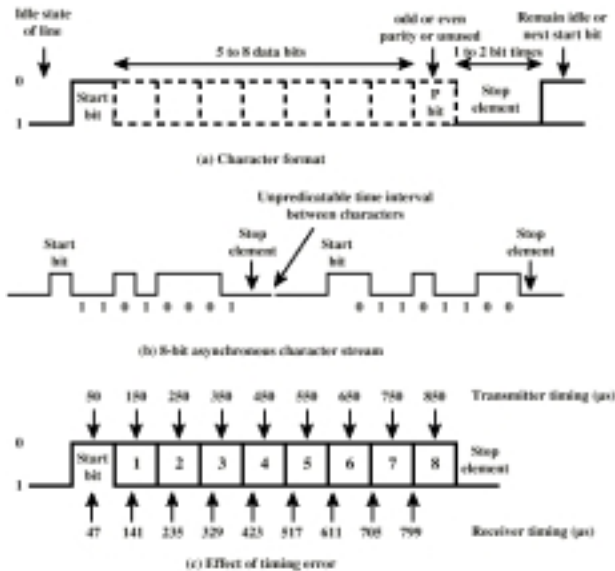
Timing Problems – Example

- ⌘ Assume sender transmits a stream of bits at a rate of 1 Mbps.
 - ☒ Bit duration = 1us
- ⌘ Assume that receiver's clock has a 1% drift over transmitter's clock.
 - ☒ First bit is sampled at 0.51us instead of 0.5us
 - ☒ Second bit is sampled at 1.52us instead of 1.5us
 - ☒ Bit#50 is sampled at 50us instead of 49.5us
- ⌘ After 50 or more samples, the receiver will be in error as it will be sampling in the wrong bit time

Asynchronous

- ⌘ Avoid timing problems by not sending long uninterrupted stream of bits.
- ⌘ Data transmitted one character at a time
 - ☒ 5 to 8 bits
- ⌘ Timing or synchronization only needs maintenance within each character
- ⌘ Resynchronize at the beginning of each new character

Asynchronous (diagram)



Asynchronous - Behavior

- ⌘ In a steady stream, interval between characters is uniform (length of stop element)
- ⌘ In idle state, receiver looks for transition 1 to 0
- ⌘ Then samples next seven intervals (char length)
- ⌘ Then looks for next 1 to 0 for next char
- ⌘ Simple and cheap
- ⌘ Overhead of 2 to 3 bits per char (~20%)
- ⌘ Good for data with large gaps (keyboard)

Synchronous - Bit Level

- ⌘ Block of data transmitted without start or stop bits
- ⌘ Clocks must be synchronized
- ⌘ Can use separate clock line
 - ☑ Good over short distances
 - ☑ Subject to impairments
- ⌘ Embed clock signal in data
 - ☑ Manchester encoding
 - ☑ Carrier frequency (analog)

Synchronous - Block Level

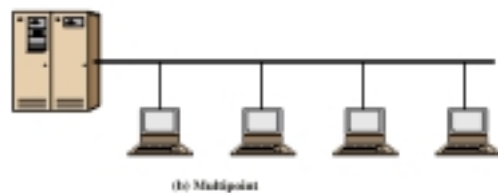
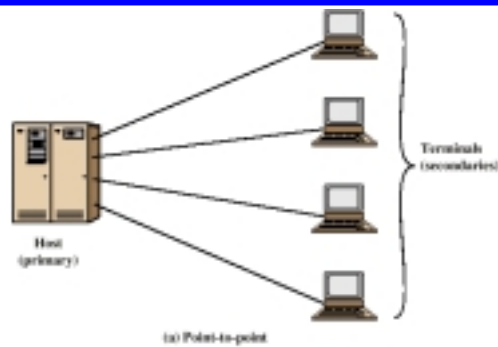
- ⌘ Need to indicate start and end of block
- ⌘ Use preamble and postamble
 - ☑ e.g. series of SYN (hex 16) characters
 - ☑ e.g. 8-bit flag 01111110
- ⌘ More efficient (lower overhead) than asynchronous



Line Configuration

- ⌘ Topology: physical arrangement of stations on medium
 - ☑ Point to point
 - ☑ Multi point
 - ☑ Computer and terminals, local area network
- ⌘ Half duplex
 - ☑ Only one station may transmit at a time
 - ☑ Requires one data path
- ⌘ Full duplex
 - ☑ Simultaneous transmission and reception between two stations
 - ☑ Requires two data paths (or echo canceling)

Traditional Configurations



Interfacing

- ⌘ Data processing devices (or **data terminal equipment, DTE**) do not (usually) include data transmission facilities
- ⌘ Need an interface called **data circuit terminating equipment (DCE)**
 - ☑ e.g. modem, NIC
- ⌘ DCE transmits bits on medium
- ⌘ DCE communicates data and control info with DTE
 - ☑ Done over interchange circuits
 - ☑ Clear interface standards required

Interfacing

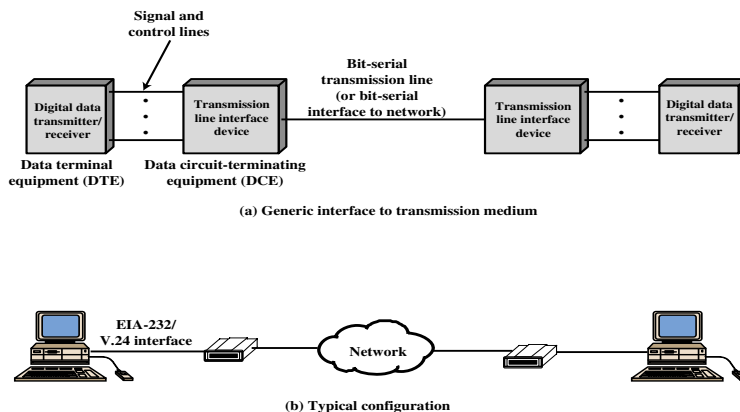


Figure 6.4 Data Communications Interfacing

Characteristics of Interface

⌘ Mechanical

- ☑ Connection plugs

⌘ Electrical

- ☑ Voltage, timing, encoding

⌘ Functional

- ☑ Data, control, timing, grounding

⌘ Procedural

- ☑ Sequence of events for transmitting data

V.24/EIA-232-F

⌘ ITU-T V.24

⌘ Only specifies functional and procedural

- ☑ References other standards for electrical and mechanical

⌘ EIA-232-F (USA)

- ☑ RS-232
- ☑ Mechanical: ISO 2110
- ☑ Electrical: V.28
- ☑ Functional: V.24
- ☑ Procedural: V.24

Mechanical Specification

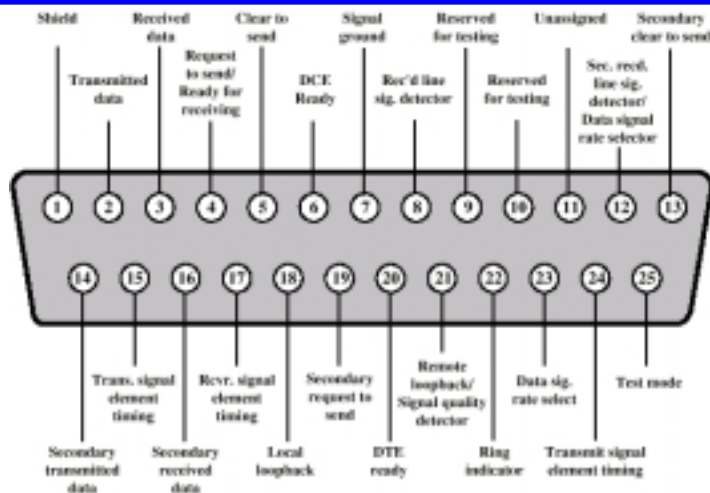


Figure 6.5 Pin Assignments for V.24/EIA-232 (DTE Connector Face)

Electrical Specification

- ⌘ Digital signals used
- ⌘ Values interpreted as data or control, depending on circuit
- ⌘ More negative than -3v is binary 1, more positive than +3v is binary 0 (NRZ-L)
- ⌘ Signal rate < 20 kbps
- ⌘ Distance < 15 m
- ⌘ For control, more negative than -3v is off, more positive than +3v is on

Functional Specification

⌘ Circuits can be grouped into four categories

- ☒ Data
- ☒ Control
- ☒ Timing
- ☒ Ground

⌘ Data group

- ☒ One data circuit in each direction: [Transmitted data \(Pin 2\)](#), [Received data \(Pin 3\)](#)
- ☒ Two secondary data circuits useful for half-duplex transmission: [Secondary Transmitted Data \(Pin 14\)](#), [Secondary Received data \(Pin 16\)](#)

Functional Specification

⌘ **16 control circuits**, 10 of which related to transmission of data over primary channel

⌘ For Asynchronous transmission, **six** of these circuits are used

- ☒ [Request to send \(Pin 4\)](#), [Clear to send \(Pin 5\)](#), [DCE Ready \(Pin 6\)](#), [DTE Ready \(Pin 20\)](#), [Ring Indicator \(Pin 22\)](#), [Received Line Signal Detector \(Pin 8\)](#)

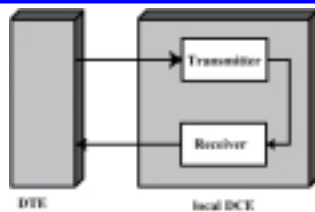
⌘ For Synchronous transmission, 4 more control signals are used

- ☒ [Signal Quality Detector \(Pin 21\)](#), [Data Signal Rate Selector \(Pin 12 & 23\)](#), [Ready for Receiving \(Pin 4\)](#)

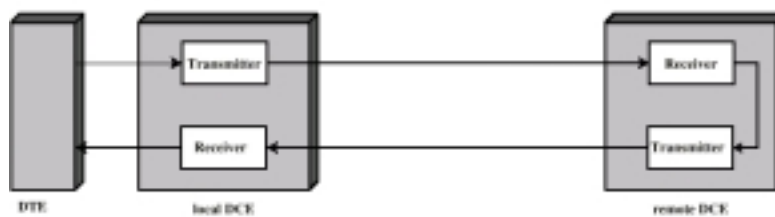
Functional Specification

- ⌘ Three control signals used to control secondary channel
 - ☑ Secondary Request to Send (Pin 19), Secondary Clear to Send (Pin 13), Secondary Received Line Signal Detector (Pin 12)
- ⌘ Three control signals used for loopback testing
 - ☑ Remote Loopback (Pin 21), Local Loopback (Pin 18), Test Mode (Pin 25)

Local and Remote Loopback



(a) Local loopback Testing



(b) Remote loopback Testing

Functional Specification

- ⌘ Three timing signals provide clock pulses for synchronous transmission
 - ☒ Transmitter Signal Element Timing (Pin 15)
 - ☒ Transmitter Signal Element Timing (Pin 24)
 - ☒ Receiver Signal Element Timing (Pin 17)
- ⌘ When DCE is sending data over **Received Data Circuit to DTE**, it sends 1-0 and 0-1 transitions on **Receiver Signal Element Timing** timed to the middle of each received data signal element.
- ⌘ When DTE is sending data to DCE either DTE or DCE can provide the synchronizing clock.

Table 6.1 V.24/EIA-232-F Interchange Circuits

V.24	EIA-232	Name	Direction to:	Function
DATA SIGNALS				
103	BA	Transmitted Data	DCE	Transmitted by DTE
104	BB	Received Data	DTE	Received by DTE
118	SBA	Secondary Transmitted Data	DCE	Transmitted by DTE
120	SCA	Secondary Received Data	DTE	Received by DTE
CONTROL SIGNALS				
105	CA	Request to send	DCE	DTE wishes to transmit
106	CB	Clear to send	DTE	DCE is ready to receive; response to Request to send
107	CC	DCE ready	DTE	DCE is ready to operate
108.2	CD	DTE ready	DCE	DTE is ready to operate
125	CE	Ring indicator	DTE	DCE is receiving a ringing signal on the channel line
109	CF	Received line signal detector	DTE	DCE is receiving a signal within appropriate limits on the channel line
110	CG	Signal quality detector	DTE	Indicates whether there is a high probability of error in the data received
111	CH	Data signal rate selector	DCE	Selects one of two data rates
112	CI	Data signal rate selector	DTE	Selects one of two data rates
133	CJ	Ready for receiving	DCE	On/off flow control
120	SCA	Secondary request to send	DCE	DTE wishes to transmit on reverse channel
121	SCB	Secondary clear to send	DTE	DCE is ready to receive on reverse channel
122	SCF	Secondary received line signal detector	DTE	Same as 109, for reverse channel
140	RL	Remote loopback	DCE	Instructs remote DCE to loop back signals
141	LL	Local loopback	DCE	Instructs DCE to loop back signals
142	TM	Test mode	DTE	Local DCE is in a test condition
TIMING SIGNALS				
113	DA	Transmitter signal element timing	DCE	Clocking signal; transitions to ON and OFF occur at center of each signal element
114	DB	Transmitter signal element timing	DTE	Clocking signal; both 113 and 114 relate to signals on circuit 103
115	DD	Receiver signal element timing	DTE	Clocking signal for circuit 104

Functional Specification
 ⌘ (See table in Stallings chapter 6)

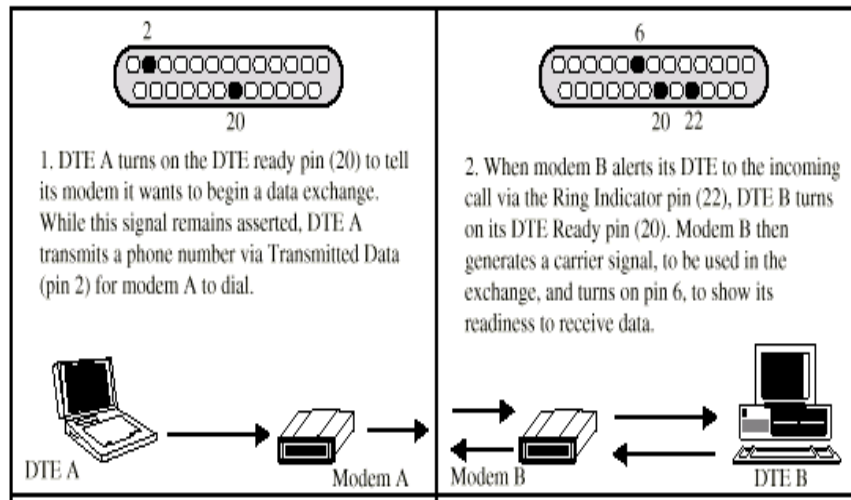
Procedural Specification

- ⌘ Example: **Asynchronous private line modem**
- ⌘ When turned on and ready, modem (DCE) asserts **DCE Ready**
- ⌘ When DTE ready to send data, it asserts **Request to Send**
 - ☒ Also inhibits receive mode in half duplex
- ⌘ Modem responds when ready by asserting **Clear to send**
- ⌘ DTE sends data over **Transmitted Data** line
- ⌘ When data arrives from remote modem, local modem asserts **Receive Line Signal Detector** and delivers data on **Received Data** line.

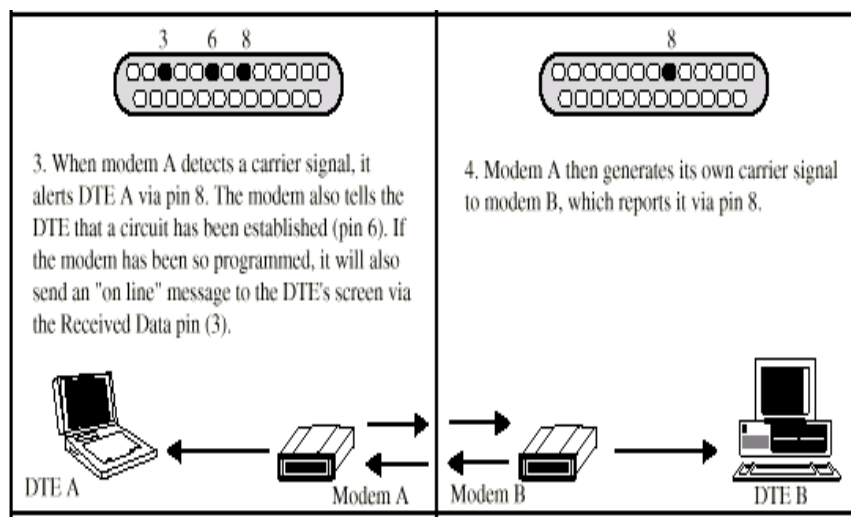
Procedural Specification

- ⌘ Asynchronous private line modem is common for connecting two devices over a short distance within a building
- ⌘ To transmit data over telephone network, two additional pins are required
 - ☒ **DTE Ready**
 - ☒ **Ring Indicator**
- ⌘ For short distances, it is possible for two DTEs to talk directly without DCEs, using **Null Modem**.

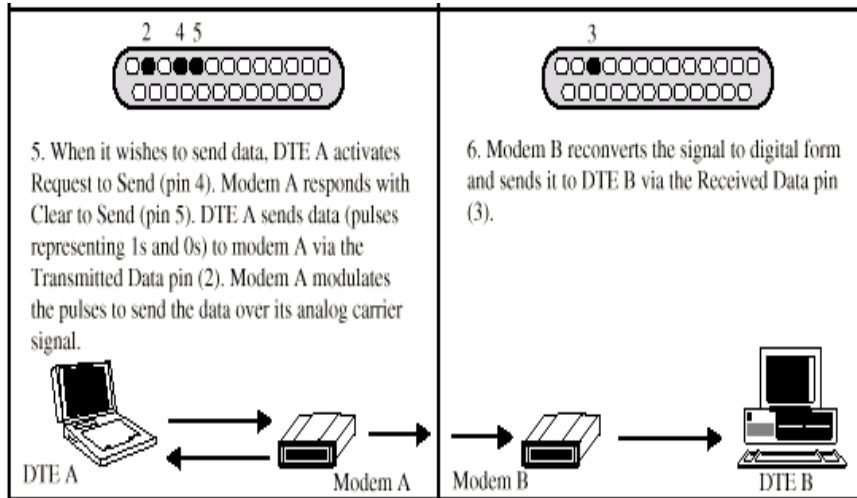
Dial Up Operation (1)



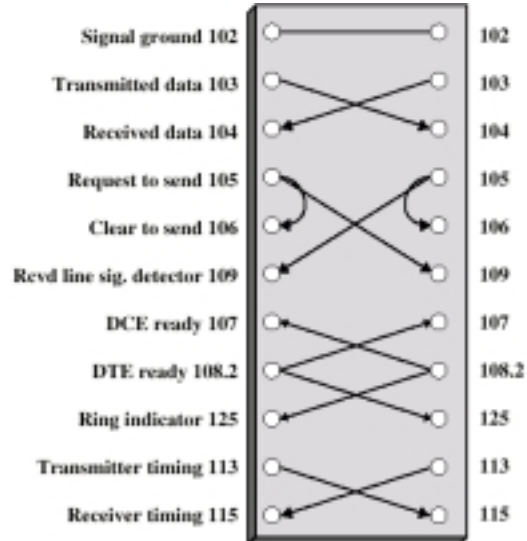
Dial Up Operation (2)



Dial Up Operation (3)



Null Modem



Integrated Services Digital Network (ISDN)

- ⌘ Support of voice and nonvoice applications
- ⌘ Support for switched and non-switched applications
- ⌘ Reliance on 64 Kbps connections
- ⌘ Provides a set of channels at a single interface
 - ☒ B channel: 64 Kbps
 - ☒ Circuit switching, packet switching, dedicate
 - ☒ D channel: 16 Kbps
 - ☒ Control signaling (call setup) and some data

ISDN Channel Structure

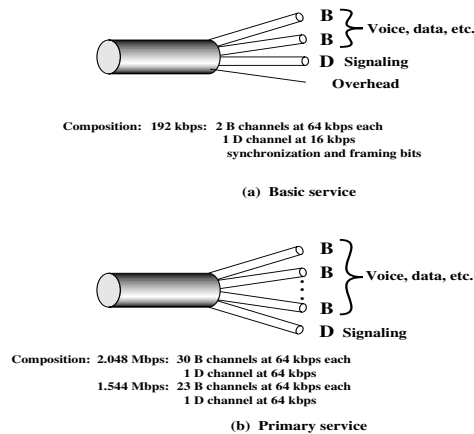


Figure A.3 ISDN Channel Structure

Conceptual View of ISDN Connection Features

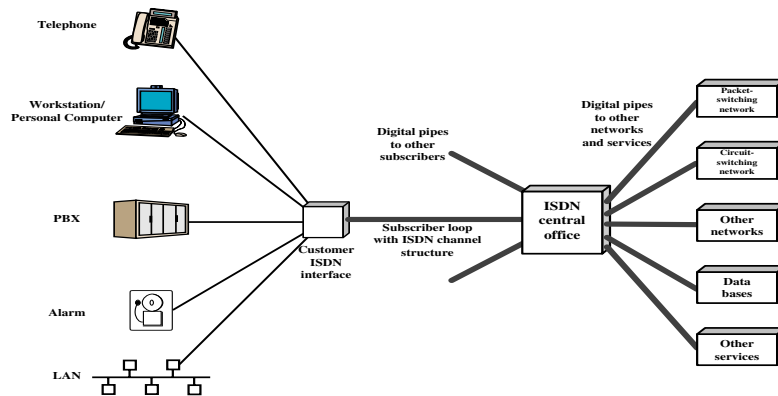


Figure A.1 Conceptual View of ISDN Connection Features

ISDN Architecture

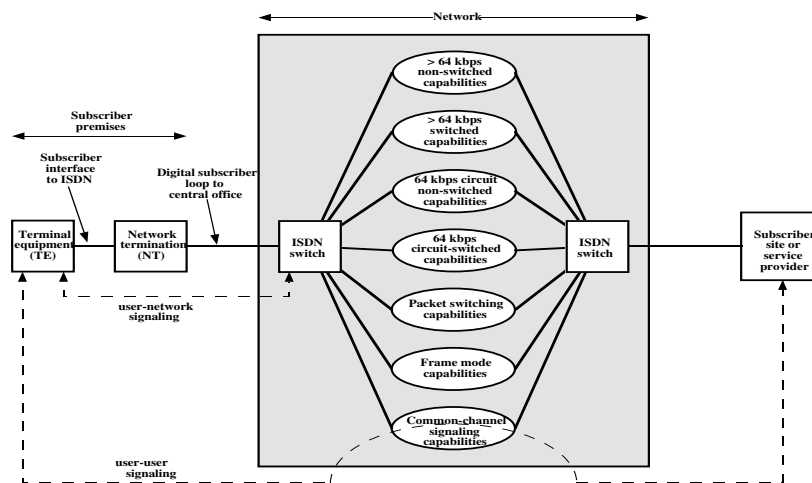
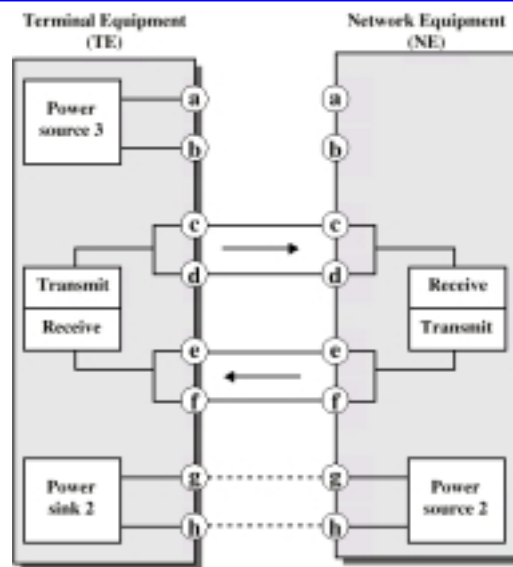


Figure A.2 ISDN Architecture

ISDN Physical Interface

- ⌘ Connection between terminal equipment (TE) and network terminating equipment (NT)
- ⌘ Physical connection defined in ISO 8877
- ⌘ Cables terminate in matching connectors with 8 contacts
- ⌘ Transmit/receive carry both data and control

ISDN Physical Interface Diagram



ISDN Electrical Specification

- ⌘ Balanced transmission
 - ☒ Carried on two lines, e.g. twisted pair
 - ☒ Signals as currents down one conductor and up the other
 - ☒ Differential signaling
 - ☒ Value depends on direction of voltage
 - ☒ Tolerates more noise and generates less
- ⌘ Unbalanced, e.g. RS-232 uses single signal line and ground)
- ⌘ Data encoding depends on data rate
- ⌘ Basic rate 192kbps uses pseudoternary
- ⌘ Primary rate uses Alternative Mark Inversion (AMI) with B8ZS (1.544 Mbps) or HDB3 (2.048 Mbps)