KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

COMPUTER ENGINEERING DEPARTMENT

COE 308-01, Term 982
HW# 4

SOLUTION

Q.1. $(1-w)\ h\ (t_i + t_c)\ +\ (1-w)\ m\ (t_i + (b/4)\ t_m)\ +\ w\ h\ t_m\ +\ w\ m\ t_m$

Q.2. Initial cache organization: 2-way, 512 sets, 16 bytes/line.
cache 1: 2-way, 512 sets, 32 bytes/line
cache 2: 2-way, 1024 sets, 16 bytes/line

(a) The following list of addresses (in decimal): 0, 16400, 32768, 0, 16400, 32768, 0, 16400, 32768, 0, 16400, 32768
gives 12 misses (all references) in cache 1 and only 3 misses in cache 2.

(b) The following list of addresses (in decimal): 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, …, 63
gives 2 misses in cache 1 and 4 misses in cache 2.

(c) Sequential accesses favor longer line sizes while random accesses, as in subroutine calls, tend to favor more sets.

Q.3. TLB: it has 128 locations. Each location has two entries. Each entry has an 18-bit real-page number and a 19-bit tag. The virtual address is divided as follows: bits 0 to 13 is the line address within a page; bits 14 to 20 is the index to TLB; bits 21 to 39 is the tag to TLB entries.

Data cache: Real address is 32-bit. Bits 0 to 13 come from bits 0 to 13 in the virtual address; bits 14 to 31 come from TLB entry as a real page address.
The real address is divided as follows: bits 0 to 1 is the byte number in the cache block; bits 2 to 9 is the set number in the cache; bits 10 to 31 is the tag.

Q.4. a) Virtual pages 2, 3, 5, 7 are not in memory. Page size = 128. Therefore, virtual addresses that are not in memory are: 256 - 383, 384 - 511, 640 – 767, 896 - 1023.

b) 384, 385, 128, fault.