Name: **Id#**

COE 308, Computer Architecture, Term 982
Quiz# 3

Date: Monday, April 12

Q1. Deduce a sequence of twelve page references for a paging system with five main memory pages, using the clock replacement algorithm, which produces each of the following characteristics:

i) The largest number of page faults.

ii) The smallest number of page faults.

Q2. A microprocessor generates a 20-bit byte address A_{19}-A_0. Design a set-associative translation look-aside buffer for the system giving details of the address translation and the number of bits in the address fields if the following applies. The page size is 1024 bytes and the TLB can handle a total of 128 page addresses. The groups of virtual addresses below are likely to appear frequently:

A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1
1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0
0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Clearly indicate your reasoning and design for minimum cost.