COE 308, Computer Architecture, Term 982
HW# 4

Due date: Monday, April 5

Q.1. In a paged system, suppose that the main memory can only hold four pages at any instant and that the following pages are requested in the order shown:

21, 4, 21, 2, 65, 33, 2, 65, 43, 4, 2, 50

(i) List the pages in the main memory after each page is transferred using the clock replacement algorithm.

(ii) List the pages in the main memory after each page is transferred assuming an optimal replacement algorithm, i.e., an algorithm that produces the minimum number of page faults.

Q.2. Deduce a sequence of page references for a paging system with eight main memory pages, using the least recently used replacement algorithm, which produces each of the following characteristics:

(i) The largest number of page faults.

(ii) The smallest number of page faults.

Q.3. Suppose that in a paged system, the main memory can hold a maximum of four pages and that the least recently used replacement algorithm will be approximated based on the use bits stored in the main memory page table. The use bits are set when a page is referenced including when a page is first loaded. The use bits are only read at page fault time and reset when read. It is assumed that the pages are scanned in the same order from page0 to page3. Given the following sequence of page references:

3, 37, 3, 89, 37, 25, 3, 57, 37, 3, 24, 25, 89, 89, 4, 4, 37, 57

(i) Using one use bit with each page entry, determine the pages removed and list the pages using one use bit approximation to the least recently used algorithm.

(ii) Suppose two bits are provided with each page entry. The first use bit is set when the page is first referenced. The second use bit is set when the page is referenced again. Determine the pages removed and list the pages using two use-bits approximation to the least recently used algorithm.

Q.4. A microprocessor generates a 20-bit byte address A_{19}-A_0. Design a set-associative translation look-aside buffer for the system giving details of the address translation and the number of bits in address fields if the following applies. The page size is to be 512 bytes and the TLB can handle a total of 256 page addresses. The groups of virtual addresses below are likely to appear frequently:

- Five addresses with A_{19} the same
- Two addresses with A_{18} through A_0 the same
- Three addresses with A_{16} through A_0 the same
- Four addresses with A_{15} through A_0 the same
- Two addresses with A_{13} through A_0 the same
- Two addresses with A_{10} through A_0 the same
- Two addresses with A_9 the same

Clearly indicate your reasoning and design for minimum cost.

Q.5. A paging system has both a virtual memory and a real address data cache, with the following characteristics:

- 40-bit virtual address
- 32-bit real address
- 8Kbyte pages
- 2-way set associative TLB with 64 entries in total
- 4-way set associative data cache with 1024 lines in total

Draw the TLB and data cache, showing the division of bits in the virtual address, real address and the number of bits in the paths between the various component parts of the system. Each line contains one 32-bit word.