KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 308-01, Term 982

Homework #4
Due Date: Monday April 5th

Q.1. Do Problem 3.6 from your book.

Q.2. Suppose you have a 2-way set associative cache of size 16 Kbytes and a line size of 16 bytes. You wish to increase the size of the cache because memory prizes have dropped since the last design was completed. You have two options - double the line size of the cache or double the number of sets. You want to estimate the performance difference of the two designs.

(a) Find a sequence of address references that produces more misses in the cache with longer line size than in the cache with more sets. Use a list at least 10 read-addresses that exhibits a specific pattern.

(b) Find a sequence of address references that produces more misses in the cache with more sets than in the cache with longer line size. Use a list at least 10 read-addresses that exhibits a specific pattern.

(c) Given your answer in (a) and (b), describe qualitatively the characteristics of an address trace (list of addresses) that determine which of the two ways to double cache size will perform better.

Q.3. Problem 4.11 page 155 from your book.

Q.4. A virtual memory system has a size of 1024 words with eight virtual pages. The physical main memory has only four pages. The main memory page table is as follows:

Virtual Page Number	Real Page Number
0	3
1	1
2	Free
3	Free
4	2
5	Free
6	0
7	Free

(i) Make a list of **ALL** virtual addresses that will cause page faults.

(ii) What is the main memory address for each of the following virtual addresses: 0, 1, 128, 1023? (all numbers are in decimal)