COE 308, Computer Architecture, Term 982
HW# 1

Due date: Wednesday, Feb. 10

Q.1. Why are memory locations organized as locations each holding one byte even in a 32-bit processor? What would be the effects of only having 32-bit locations on the design of the system (i.e. not having byte locations)? What are the advantages and disadvantages?

Q.2. Suppose technology has advanced to enable 64 RISC processors to be fabricated on one chip or a single superscalar RISC processor with a scalarity of 64 (capable of executing 64 instructions simultaneously) to be fabricated on one chip. Discuss the two options and write a report recommending one.

Q.3. Why was microprogramming invented? Discuss whether it is currently used or not?

Q.4. Name one memory addressing mode usually not found in RISC processors. Name two other characteristics common to most RISCs.

Q.5. A 16-bit microprocessor has a 32-bit databus and a 1 Mbyte memory. Show the memory organization and the processor-memory interface such that the processor will be able to access two 16-bits simultaneously and possibly from different locations.

Q.6. Express the following numbers in binary:

(i) 123.22

(ii) 555.75

Q.7. Express the following numbers in both sign-magnitude and 2's complement representations:

(i) –1111

(ii) –321

Q.8. Perform the following operations twice, once for a sign-magnitude representation and once for 2's complement representation. Indicate in your answer when an overflow occurs:

(i) 010101 + 001011

(ii) 110111 - 111001

Q.9. Discuss the advantages and disadvantages of the sign-magnitude and 2's complement representations. Show the architectures of an 8-bit adder/subtractor for both sign-magnitude and 2's complement representations, and compare the two architectures. Assume that the two numbers to be added or subtracted will be held in two registers, A

and B, and that the result will be stored in register C. Also, assume that the subtraction operation can be performed as either A-B or B-A.

Q.10. Describe the logic required for detecting an overflow condition for both sign-magnitude and 2's complement representations when performing addition/subtraction operations.