March 16, 1999

COMPUTER ENGINEERING DEPARTMENT

COE 308

COMPUTER ARCHITECTURE

Major Exam I

Second Semester (982)

Time: 8:00-10:00 PM

Student Name : _____

Student ID. : _____

Question	Max Points	Score
Q1	15	
Q2	20	
Q3	10	
Q4	15	
Q5	15	
Q6	15	
Q7	10	
Total	100	

Dr. Aiman El-Maleh

[15 Points]

(Q1) Given two n-bit numbers $\mathbf{A=A_{n-1}\ A_{n-2}\ .\ .\ .\ .A_0}$ and $\mathbf{B=\ B_{n-1}\ B_{n-2}\ .\ .\ .\ .B_0}$, where $\mathbf{A_{n-1}}$ and $\mathbf{B_{n-1}}$ represent the sign bits for A and B, respectively. Assume that when an adder/subtractor receives a 0 on the input **OP**, it performs an addition operation, otherwise it performs a subtraction operation.

(a) Show the logic to indicate the presence of an overflow for sign-magnitude addition/subtraction of the two numbers.

(b) Show the logic to indicate the presence of an overflow for 2`s complement addition/subtraction of the two numbers.

(c) Show that $\mathbf{A * (2^n + 2^{n-1} + 2^{n-2} + \ldots + 2^{n-k}) = A * 2^{n+1} - A * 2^{n-k}}$

[20 Points]

(Q2) Given the numbers **A=-12** and **B=-5** represented in two`s complement format assuming 5-bit words.

(a) Use the Booth algorithm to perform the multiplication operation **A*B**. Show all the steps cycle by cycle.

(b) Perform the division operation **A/B**. Determine the quotient and remainder, and show all the steps cycle by cycle.

[10 Points]

(Q3) Suppose that a computer receives real numbers in the range **0 to 63**. It is required to store the received numbers with **a minimum precision of 0.25**.

(a) Show a **10-bit** floating-point format for representing the above numbers. Assume that **normalized numbers** are in the form **0.1bb. . .b,** where b is either a 0 or 1.

(b) Show the representation of the numbers **0.30** and **62.9**, and the relative error in their representation using the format you design in (a).

[15 Points]

(Q4) A Pentium microprocessor has a **32 Mbyte main memory**, a **4 Kbyte instruction cache**, and a **4 Kbyte data cache**.

(a) Show the memory organization and the processor-main memory interface such that the processor will be able to access from the main memory two 32-bits simultaneously and possibly from different locations.

(b) Assuming the following:

- Main memory word access time $\mathbf{t_m=200ns}$,
- Instruction cache word access time $\mathbf{t_{ci}=20ns}$,
- Data cache word access time $\mathbf{t_{cd}=25ns}$,
- Instruction hit ratio $\mathbf{h_i=0.9}$,
- Data hit ratio $\mathbf{h_d=0.8}$,
- Average number of executions per data word $\mathbf{n_d=2}$,
- Average number of executions per instruction word $\mathbf{n_i=4}$,
- **30%** of operations are data read/write operations,

Compute the **word average access time** assuming the memory interleaving organization in (a). Note that two different words can be accessed from the main memory in 200ns.

[15 Points]

(Q5) A microprocessor has a **64-bit data bus**, a **32 Mbyte main memory**, and an **8 Kbyte data cache**. It is assumed that two words, possibly from different locations, are transferred simultaneously between the processor, main memory, and cache. Show the cache organization including the number of bits in each field of the address and the valid bits in the cache for the following:

(a) **Full-Associative** mapping with a line size of 8 words.

(b) **Direct** mapping with a line size of 8 words

(c) **Four-way set-associative** mapping with a line size of 2 words.

[15 Points]

(Q6) A computer system has a main memory with an access time $\mathbf{t_m}$, and a cache with an access time $\mathbf{t_c}$ and a hit ratio **h**. Assume that the time to transfer a line from/to the cache is $\mathbf{t_m}$, and the fraction of write references is **w**.

(a) Determine the average access time assuming a write-through mechanism with fetch on write policy.

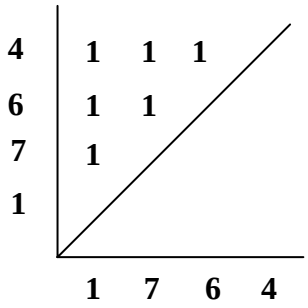
(b) Determine the average access time assuming a simple write-back policy.

(c) Determine the conditions under which a write-through policy will have a larger average access time than the simple write-back policy, given that the hit ratio is the same in both cases.

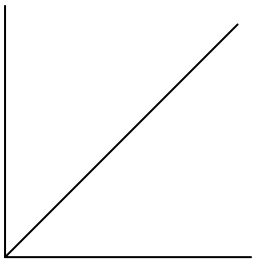
[10 Points]

(Q7) Assume that a reference matrix method is used to implement the least recently used algorithm in a cache that holds four lines. Given that the figure below indicates the current state of the reference matrix, show what changes would occur in the reference matrix if the following sequence of addresses is requested:

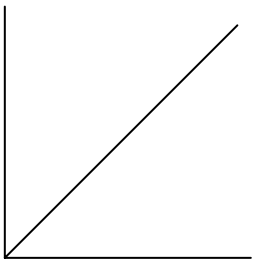
6 3 2 7 4



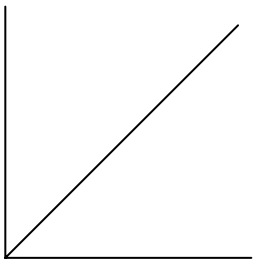
Initial
LRU=



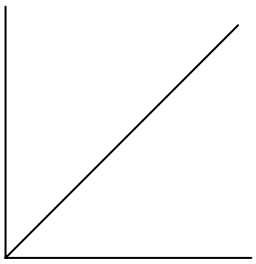
Line=6
LRU=



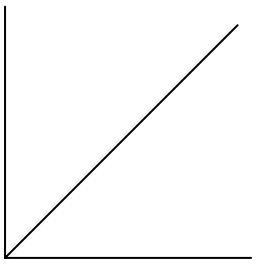
Line=3
LRU=



Line=2
LRU=



Line=7
LRU=



Line=4
LRU=