

Name: KEY

Id#

COE 205, Term 091

Computer Organization & Assembly Programming
Quiz# 6

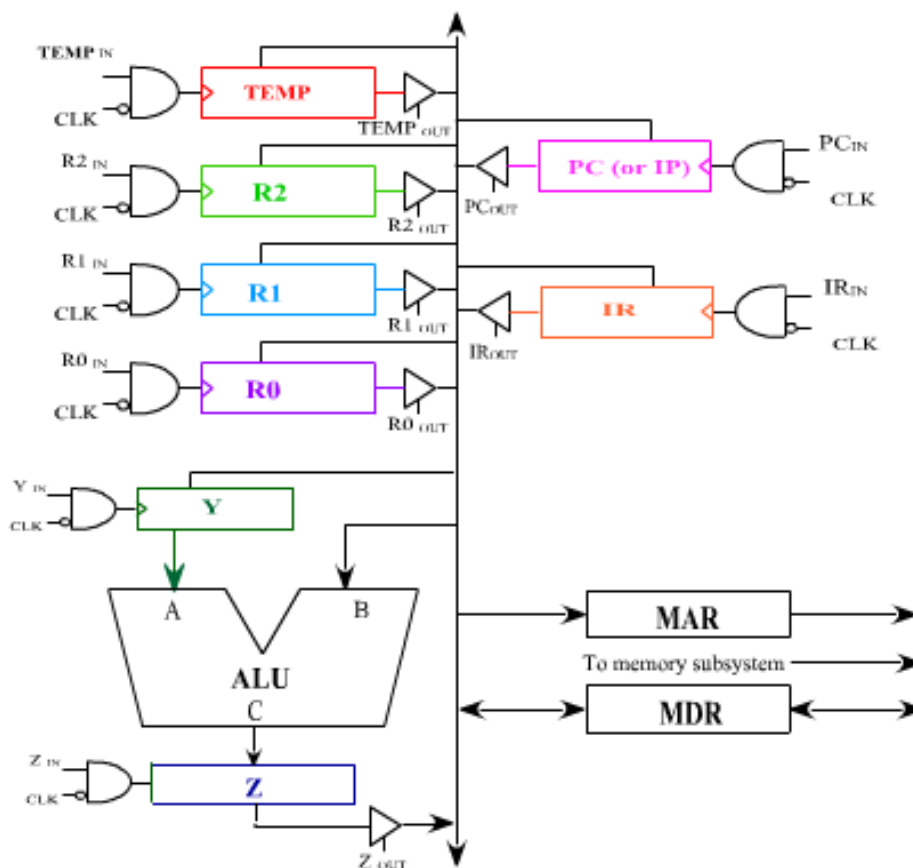
Q1. Consider the one-bus CPU organization shown below. Assume that the CPU has only three general registers, namely R0, R1, and R2 and it has also a temporary register Temp. Furthermore, assume that the ALU can perform any of the following four functions based on the control signals $f1$, $f2$, $f3$, and $f4$, as shown below:

$f1: C=A+B;$

$f2: C=A-B;$

$f3: C=A+1;$

$f4: C=A-1;$



(i) T₁ PC_{out}, MAR_{in}, Read, Yin
 T₂ f₃, Z_{in}
 T₃ Z_{out}, PC_{in}, WMFC
 T₄ MDR_{out}, IR_{in}

(ii) a. JE label

T₅ PC_{out}, Yin, if (ZF=0) END
 T₆ IR_{out}, f₁, Z_{in}
 T₇ Z_{out}, PC_{in}, END

b. SUB J, 5

T₅ IR_{out}, MAR_{in}, Read, WMFC
 T₆ MDR_{out}, Yin
 T₇ IR_{out}, f₂, Z_{in}
 T₈ Z_{out}, MDR_{in}, Write, WMFC
 T₉ END

c. XCHG R1, R2

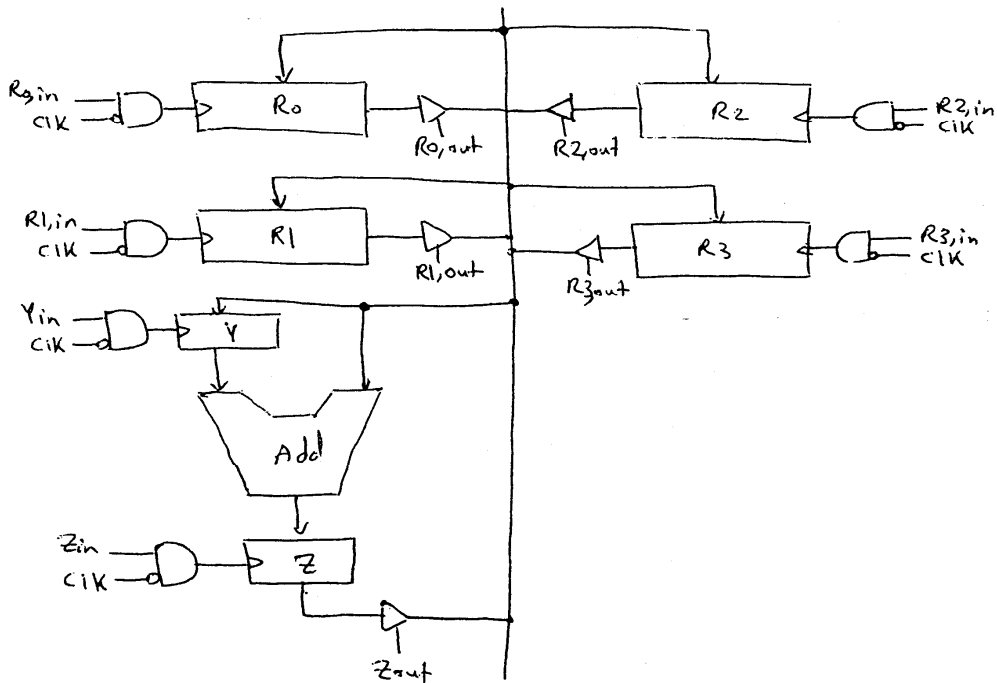
T₅ R_{1out}, Temp_{in}
 T₆ ~~R_{2out}~~, R_{1in}
 T₇ Temp_{out}, R_{2in}, END

d. Loop label

T₅ R_{0out}, Yin
 T₆ f₄, Z_{in}
 T₇ Z_{out}, R_{0in}, if (ZF=1) end
 T₈ PC_{out}, Yin
 T₉ IR_{out}, f₁, Z_{in}
 T₁₀ Z_{out}, PC_{in}, end

(iii) PC_{in} = T₃ + JE · T₇ + Loop · T₁₀

Q2. It is required to design a data path to execute the following two types of instructions: *MOV Rdst, Rsrc* and *ADD Rdst, Rsrc*, where *Rsrc* and *Rdst* can be either R0, R1, R2, or R3. Show the data-path design and indicate all the signals needed to control it. Note that you only need to show the interconnection of the registers with the adder i.e., there is no need to show the PC, IR, MAR and MDR registers.



Note that the signals $R_{0,out}$, $R_{1,out}$, $R_{2,out}$, and $R_{3,out}$ are derived from the signals $R_{src,out}$, $R_{dst,out}$ and the content of IR. Similarly, the signals $R_{0,in}$, $R_{1,in}$, $R_{2,in}$, and $R_{3,in}$ are derived from the signal $R_{dst,in}$ and the content of IR.