Name: KEY **Id#**

COE 205, Term 062

Computer Organization & Assembly Programming

Quiz# 2

Date: Saturday, March 17, 2007

Q1. Fill the blank in each of the following questions:

1. The CPU is interfaced with memory and input/output devices through the **address bus**, **data bus** and **control bus**.

2. The CPU consists mainly of the **data path** unit and the **control** unit.

3. If the clock period of a CPU is 0.5 ns, then its clock frequency is **2 GHz**.

4. A CPU with a 32-bit address bus has **4 GByte** physical address space.

5. With a **data bus size** equal to **64 bits**, the maximum number of bytes that is transferred between the CPU and memory per a read/write cycle is **8** Bytes.

6. The **RAM** is faster than **hard disk** and slower than **cash memory**.

7. The **disk access time** is equal **seek time + rotation latency + transfer time**.

8. The size of the **address bus** in the **8086** processor is **20** bits while in the **Pentium IV** Processor it is **36** bits.

9. The size of the **data bus** in the **8086** processor is **16** bits while in the **Pentium IV** Processor it is **64** bits.

10. CISC stands for **Complex Instruction Set Computer** while RISC stands for **Reduced Instruction Set Computer.**

11. The IA-32 registers consist of **8** 32-bit general-purpose registers, **6** 16-bit segment registers, the **EIP** register and the **EFLAGS** register.

12. Adding the following two 8-bit numbers FE+D5 has the following values on the flags: CF=**1**, ZF=**0**, SF=**1**, AF=**1**, PF=0, OF=0.

    FE + D5 = D3 = 1101 0011

13. The **Instruction Register (IR)** holds the fetched instruction to be executed.

14. The **Instruction Pointer (IP)** register holds the address of the next instruction to be fetched from memory.

15. After reading an instruction whose size is **32 bits**, the **instruction pointer** is incremented by **4**.

16. The instruction fetch-execute cycle can be divided into five stages: **instruction fetch, instruction decode, operand fetch, execute,** and **write back result**

17. **Pipelining** makes its possible to start an instruction before completing the execution of previous one.

18. In real address mode, the staring address of segment#F005 is **F0050** and the maximum ending address is FFFFF.

    F0050+0FFFF = 0004F. Since it exceeds the largest address, the maximum address allowed is FFFFF.

19. In real address mode with a logical address given as 2305:15F9, the linear address is **24649**.

    23050 + 015F9 = 24649

20. In protected mode, linear address is translated to physical address using **Paging.**