Name: **Id#**

COE 205, Term 091

Computer Organization & Assembly Programming

Quiz# 2

Date: Monday, Nov. 9, 2009

Q1. Fill the blank in each of the following:

1. The 8086 processor is a _____ bit machine with an address bus of _____ bits and a data bus with _____ bits.

2. The Pentium 4 processor is a _____ bit machine with an address bus of _____ bits and a data bus with _____ bits.

3. _____ are based on having small and simple instruction set and have fixed width instructions.

4. _____ are based on having large and complex instruction set and have variable width instructions.

5. The IA-32 has _____ general purpose registers, _____ segment registers, _____ and _____.

6. Programmers can access the registers _____ either as 32-bit registers, or can access their 16-bit and 8-bit parts.

7. The overflow flag is set when _____.

8. The carry flag is set when _____.

9. The sign flag is set when _____.

10. The zero flag is set when _____.

11. The parity flag is set when _____.

12. The address of the instruction to be fetched is stored in a register called _____.

13. Given a 5-stage pipeline where each stage executes in one clock cycle, a clock cycle time of 1 ns (i.e. 10^{-9} sec), the time needed for executing 1 billion instructions without any pipeline stall is nearly _____ sec.

14. Suppose that the memory addresses occupied so far is from 00000 to 020F1. The first available free segment is segment#_____.

15. Assume that DS=12FF, CS=E6F0, ES=F135, SS=ABCD, IP=0016, and SI=526F. The physical address of the next instruction to be fetched from memory in real address mode is _____.

16. In real address mode, the starting physical address for segment number 20h is _____and the ending physical address is _____.

17. In protected mode, the logical address consists of _____and _____.

18. In protected mode, the segment unit translates logical address to linear address using _____ and the _____unit translates linear address to physical address.