Name: **Id#**

COE 205, Term 062

Computer Organization & Assembly Programming

Quiz# 2

Date: Saturday, March 17, 2007

Q1. Fill the blank in each of the following questions:

1. The CPU is interfaced with memory and input/output devices through the _____, _____ and _____.
2. The CPU consists mainly of the _____ unit and the _____ unit.
3. If the clock period of a CPU is 0.5 ns, then its clock frequency is _____.
4. A CPU with a 32-bit address bus has _____ physical address space.
5. With a **data bus size** equal to **64 bits**, the maximum number of bytes that is transferred between the CPU and memory per a read/write cycle is _____ Bytes.
6. The **RAM** is faster than _____ and slower than _____.
7. The **disk access time is equal** _____ + _____ + _____.
8. The size of the **address bus** in the **8086** processor is _____ bits while in the **Pentium IV** Processor it is _____ bits.
9. The size of the **data bus** in the **8086** processor is _____ bits while in the **Pentium IV** Processor it is _____ bits.
10. CISC stands for _____ while RISC stands for _____.

11. The IA-32 registers consist of _____ 32-bit general-purpose registers, _____ 16-bit segment registers, the _____ register and the _____register.

12. Adding the following two 8-bit numbers FE+D5 has the following values on the flags: CF=_____, ZF=_____, SF=_____, AF=_____, PF=_____, OF=_____.

13. The _____ register holds the fetched instruction to be executed.

14. The _____ register holds the address of the next instruction to be fetched from memory.

15. After reading an instruction whose size is **32 bits**, the **instruction pointer** is incremented by _____.

16. The instruction fetch-execute cycle can be divided into five stages: **_____, _____, _____, _____,** and **_____**.

17. **_____** makes its possible to start an instruction before completing the execution of previous one.

18. In real address mode, the staring address of segment#F005 is _____ and the maximum ending address is _____.

19. In real address mode with a logical address given as 2305:15F9, the linear address is **_____**.

20. In protected mode, linear address is translated to physical address using **_____**.