

Name: KEY

Id#

COE 205, Term 023
Computer Organization & Assembly Programming

Quiz# 1

Date: Tuesday, July 8, 2003

Q1. Fill the blank in each of the following questions:

- i. The **Instruction Pointer** register holds the address of the next instruction to be fetched from memory.
- ii. The **Instruction** register holds the fetched instruction to be executed.
- iii. The **Memory Address** register is connected to the address bus in the CPU memory interface.
- iv. The **Memory Data** register is connected to the data bus in the CPU memory interface.
- v. The Instruction Set Architecture (ISA) of a computer consists of **the instruction set, the machine's memory, and the programmer's accessible registers.**
- vi. The size of the address bus in the 8086 processor is **20** bits while in the Pentium Processor it is **32** bits.
- vii. The size of the data bus in the 8086 processor is **16** bits while in the Pentium Processor it is **64** bits.
- viii. Reading an instruction from Memory is performed in the **fetch** phase.
- ix. Reading operands from Memory is performed in the **execute** phase.
- x. Incrementing the Instruction Pointer is performed in the **fetch** phase.
- xi. Decoding an instruction is performed in the **execute** phase.