

Name:

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COE 205, Term 032
Computer Organization & Assembly Programming

Quiz# 1

Date: Tuesday, Feb. 24, 2004

Q1. Fill the blank in each of the following questions:

- i. The _____ register holds the address of the next instruction to be fetched from memory.
- ii. The _____ register holds the fetched instruction to be executed.
- iii. The _____ register is connected to the address bus in the CPU memory interface.
- iv. The _____ register is connected to the data bus in the CPU memory interface.
- v. The Instruction Set Architecture (ISA) of a computer consists of _____, _____, and _____.
- vi. The size of the address bus in the 8086 processor is _____ bits while in the Pentium Processor it is _____ bits.
- vii. The size of the data bus in the 8086 processor is _____ bits while in the Pentium Processor it is _____ bits.
- viii. Reading an instruction from Memory is performed in the _____ phase.
- ix. Reading operands from Memory is performed in the _____ phase.
- x. Incrementing the Instruction Pointer is performed in the _____ phase.
- xi. Decoding an instruction is performed in the _____ phase.