

HW#6Q1. Fetch Phase:

T1 PCout, MARin, Read, Clear Y, Cin=1, Add, Zin
 T2 Zout, PCin, WMFC
 T3 MDRout, IRin ; 1st part of the instruction
 T4 PCout, MARin, Read, Clear Y, Cin=1, Add, Zin
 T5 Zout, PCin, WMFC
 T6 MDRout, IRin ; 2nd part of the instruction

(a) ADD R1, 10

T7 R1out, Yin
 T8 IRout, ADD, Zin
 T9 Zout, R1in, END

(b) ADD R1, var1

T7 IRout, MARin, Read
 T8 R1out, Yin, WMFC
 T9 MDRout, Add, Zin
 T10 Zout, R1in, END

(c) Add [var1], R1

T7 IRout, MARin, Read, WMFC
T8 Rlout, Yin
T9 MDRout, MARin, Read, WMFC
T10 MDRout, Add, Zin
T11 Zout, MDRin, write, WMFC
T12 End

(d) JNZ label 4

T7 PCout, Yin, if ZF=1 END
T8 IRout, Add, Zin
T9 Zout, PCin, End

Q2 Memory access is synchronous

(c) Add [var1], R1

T7 IRout, MARin, Read
T8 Rlout, Yin
T9
T10 MDRout, MARin, Read
T11
T12
T13 MDRout, Add, Zin
T14 Zout, MDRin, write
T15
T16
T17 END

Q3 ADD R1, 10

- Two-bus organization :

Fetch	T1	PCout, ALU (C=B), MARin, Read
	T2	PCout, ALU (C=B+1), PCin, WMFC
	T3	MDRout, ALU (C=B), IRin, 1st part
	T4	PCout, ALU (C=B), MARin, Read
	T5	PCout, ALU (C=B+1), PCin, WMFC
	T6	MDRout, ALU (C=B), IRin, 2nd part
	T7	R1out, ALU (C=B), Ain
	T8	IRout, ALU (C=A+B), R1in, END

$$\begin{aligned} \% \text{ Speedup} &= \frac{T_{1\text{-bus}} - T_{2\text{-bus}}}{T_{2\text{-bus}}} \times 100 \\ &= \frac{9\tau_1 - 8\tau_2}{8\tau_2} \times 100 \end{aligned}$$

$$\begin{aligned} \tau_1 &= \tau_{\text{tristate}} + \tau_{\text{bus}} + \tau_{\text{ALU}} + \tau_{\text{FF}} \\ &= 5\text{ns} + 5\text{ns} + 14\text{ns} + 6\text{ns} = 30\text{ns} \end{aligned}$$

$$\begin{aligned} \tau_2 &= \tau_{\text{tristate}} + \tau_{\text{bus}} + \tau_{\text{ALU}} + \tau_{\text{bus}} + \tau_{\text{FF}} \\ &= 5\text{ns} + 5\text{ns} + 14\text{ns} + 5\text{ns} + 6\text{ns} = 35\text{ns} \end{aligned}$$

$$\Rightarrow \% \text{ Speedup} = \frac{9 \times 30\text{ns} - 8 \times 35\text{ns}}{8 \times 35\text{ns}} \times 100 = -3.6\%$$

This means that for this instruction and propagation delay values given, the single-bus organization is faster.

- Three-bus organization:

Fetch

{	T ₁	PCout, MARin, B, Read, ALU (C=B+1), PCin, WMFC
	T ₂	MDRout, ALU (C=B), IRin; 1st part
	T ₃	PCout, MARin, B, Read, ALU (C=B+1), PCin, WMFC
	T ₄	MDRout, ALU (C=B), IRin; 2nd part
	T ₅	Rlout, B, IRout, ALU (C=A+B), Rlin, END

$$\% \text{ speedup} = \frac{T_{1\text{-bus}} - T_{3\text{-bus}}}{T_{3\text{-bus}}} \times 100$$

$$= \frac{9\tau_1 - 5\tau_3}{5\tau_3} \times 100$$

$$\tau_1 = 30 \text{ ns}$$

$$\tau_3 = \tau_{\text{write}} + \tau_{\text{bus}} + \tau_{\text{ALU}} + \tau_{\text{bus}} + \tau_{\text{ff}} = 35 \text{ ns}$$

$$\Rightarrow \% \text{ speedup} = \frac{9 \times 30 \text{ ns} - 5 \times 35 \text{ ns}}{5 \times 35 \text{ ns}} \times 100 = 54.3\%$$

Q4

(a)

$$\text{Add} = T_1 + T_4 + \text{Inst 1} \cdot T_8 + \text{Inst 2} \cdot T_9 + \text{Inst 3} \cdot T_{10} + \text{Inst 4} \cdot T_8$$

$$\text{END} = \text{Inst 4} \cdot T_9 + \text{Inst 2} \cdot T_{10} + \text{Inst 3} \cdot T_{12} + \text{Inst 4} (T_9 + T_7 \cdot 2F)$$

(b) Horizontal control word:

PCin, PCout, MARin, MDRout, IRin, IRout, Yin, Zin, Zout, Rlin, Rlout, Cn, Clear Y, Add, Read, Write, WMFC, END, MDRin