KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 993 Lectures

	Date	Topics	Ref.	Lab
1	U 11/6	Syllabus. Introduction. The general purpose machine, Views of the computer: the user`s view, the machine/assembly language programmer`s view, the computer architect`s view.	Handout	
2	M 12/6	***Computer structure***: Instruction Set Architecture, CPU organization, memory organization, and I/O.	2.2, Handout	
	M 12/6			Introduction, using MASM
3	T 13/6	***Info. Representation***: Binary, Octal, Hex., 2`s complement representation. 2`s complement addition/subtraction, range.	App. B	
4	W 14/6	***Assembly Concepts***: Overflow, ASCII characters, assembly directives and instructions. **(HW#1 Distributed**)	App. B, 2.1, 2.3	
5	TH 15/6	***Assembly Concepts***: declaring variables (DB, DW, DD), constants (EQU), and arrays (DUP), type and size of information. 8086 memory.	2.3, 2.5, handout	
6	S 17/6	***Assembly Concepts:*** Assembly instruction format. I/O using DOS functions. INT 21H with functions 1, 2, 8, 9, and A. OFFSET operator.	3.3	
	S 17/6			I/O
7	U 18/6	***8086 registers and memory segmentation:*** list of 8086 registers and their use. Code, data, and stack segments. Offset address and physical address. LEA inst. **(HW#1 Collected**)	3.1, 3.2 handout	
8	M 19/6	***8086*** Flags (Carry, Zero, Sign, Overflow, Parity, Auxiliary). ***Assembly Concepts:*** Addressing modes. **(Quiz#1)**	3.1, 4.3, handout	
	M 19/6			Segmentation & addressing modes
9	T 20/6	***Assembly Concepts:*** Addressing modes. Instruction types, MOV instruction. Data type, accessing memory. **(HW#2 Distributed**)	4.3, handout	
10	W 21/6	***8086 instructions***: MOV with indexing, XCHG, ADD, SUB, ADC, SBB, INC, DEC.	3.2, handout	
11	S 24/6	***8086 instructions***: NEG, CMP, CBW, CWD, MUL, IMUL **(HW#2 Collected**)	3.2, handout	
	S 24/6			Indexing,

				data manipulation
12	U 25/6	***8086 instructions:*** DIV, IDIV **(Quiz#2) (HW#3 Distributed**)	3.2, handout	
13	M 26/6	***8086 instructions:*** Logical instructions, AND, OR, XOR, NOT, TEST.	4.1, handout	
	M 26/6			Arithmetic, logical
14	T 27/6	***8086 instructions:*** Shift instructions, SHR, SAR, SHL/SAL.	4.1, handout	
15	W 28/6	***8086 instructions***: Rotate instructions, ROR, ROL, RCL, RCR. **(HW#3 Collected**)	4.1, handout	
16	S 1/7	***8086 instructions:*** Jump instructions. Conditional jumps, JZ, JNZ, JE, JNE, JS, JNS, JO, JNO, JP, JNP. **(Exam I)**	3.5, handout	
	S 1/7			Shift, rotate, jump, loop
17	U 2/7	***8086 instructions:*** Conditional jumps: signed and unsigned instructions. LOOP, LOOPE, LOOPNE.	3.5, handout	
18	M 3/7	***8086 instructions:*** Stack operations: PUSH, POP. Subprograms and Macros. The execution of CALL, RET.	2.4, 3.4, 4.2, 4.4 handout	
	M 3/7			Subroutines & macros
19	T 4/7	***8086 instructions:*** Parameter passing in subroutines and macros. **(HW#4 Distributed**)	3.4, 4.2, 4.4 handout	
20	W 5/7	***8086 instructions:*** String instructions, CLD, STD, MOVS.	Handout	
21	S 8/7	***8086 instructions:*** SCAS, CMPS, LODS, STOS, SCAS String instructions prefixes: REP, REPE, REPNE.	Handout	
	S 8/7			String instructions
22	U 9/7	I/O instructions, IN, OUT. ***Interrupts:*** hardware and software interrupts, INT instruction, interrupt type, interrupt vector table.	Handout	
23	M 10/7	***Interrupts:*** 8086 interrupt processing. **(HW#4 Collected**)	Handout	
	M 10/7			Video memory
24	T 11/7	***Computer Structure***: Bus system, data bus, address bus, control bus (command, timing, arbitration). **(Quiz#3)** **(HW#5 Distributed**)	5.1, handout	
25	W 12/7	***Computer Structure***: memory hierarchy, random access, access time vs. cycle time, DRAM, SRAM.	5.1, handout	
26	S 15/7	***Computer Structure***: external memory, disks, direct access,	5.1,	

		average access time and transfer rate. Tapes, sequential access. CD-ROM. **(HW#5 Collected**)	handout	
27	U 16/7	Processor Design: Datapath and Control unit, register transfer, fetch-execute cycle.	Handout	
28	M 17/7	Single-bus CPU. Register transfer timing. **(Exam II)**	Handout	
	M 17/7			Interrupts
29	T 18/7	***Memory-CPU interface:*** Synchronous vs. Asynchronous.	Handout	
30	W 19/7	Single-Bus CPU: Execution of add instruction, execution of unconditional and conditional branch instructions.	Handout	
31	S 22/7	***Performance considerations:*** 2-bus CPU & 3-bus CPU.	Handout	
	S 22/7			Using the mouse
32	U 23/7	***Control unit design:*** hardwired control unit organization, generation of control signals.	Handout	
33	M 24/7	CPU-Memory interaction circuit design, practical aspects of circuit implementation. ***An example of a simple CPU design.***	Handout	
	M 24/7			Serial Communication
34	T 25/7	Microprogrammed control: microprogrammed control unit operation, microroutines for add & branch on negative. **(HW#6 Distributed**)	Handout	
35	W 26/7	Microprogrammed control: microprogramed control unit with conditional branching, microinstruction format:field-encoded.	Handout	
36	S 29/7	Horizontal vs. Vertical control store, Nanocoding, Microcode branching example. ***Microprogram Example***: Add instruction with addressing modes. **(HW#6 Collected**)	Handout	
	S 29/7			Project
37	U 30/7	Microinstruction sharing, multiway branching, wide branch addressing, Bit Oring. **(Quiz#4)**	Handout	
38	M 31/7	Microinstruction sequencing, Microinstruction format:Example, Control signal generation. Improving performance of microprogrammed control unit.	Handout	