KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 043 Lecture Breakdown

	Date	Topics	Ref.	Lab
	S 2/7			Introduction, using MASM
1	S 2/7	Syllabus. **Introduction**. Computer System, CPU, Memory, CPU-Memory Interface, Data Bus, Address Bus, Control Bus. Memory Hierarchy: RAM, Cache.	Chapter1 (Organization) & Chapter 1 (Assembly)	
2	U 3/7	Registers. Machine Language, Assembly Language. Instruction Formats, Opcode, Operands. Stored Program Concept, **Fetch-Execute Cycle**, Instruction Pointer. Instruction Register.	Chapter1 (Organization) & Chapter 1 (Assembly)	
	M 4/7			Introduction, using MASM
3	M 4/7	**Why assembly language programming**. Data Typing in High Level and Assembly Language, Assembler, Linker, Debugger. Programmer's view of the computer, **Instruction Set Architecture** (ISA). i8086 processor characteristics, Control Unit & Datapath. Interfacing the CPU to memory & I/O. Types of Buses. One and Two-bus Architectures.	Chapter1 (Organization) & Chapter 1 (Assembly)	
4	T 5/7	**Number representation**: Binary, Octal, Hex. base conversion, fraction representation, unsigned and signed numbers. Sign-magnitude, 1's complement, 2's complement.	Appendix A & E (Assembly)	
5	W 6/7	Ranges of unsigned and signed number representation. Overflow detection for unsigned and signed numbers. **Character Representation**. ASCII Code. Even and Odd Parity.	Appendix A & E (Assembly)	
	S 9/7			Assembly Format &Data Representation
6	S 9/7	**Assembly language syntax & Program Structure**. Variable Declaration: DB,	Chapter 3 & Section 12.5	

		DW. **(Quiz#1)**	(Assembly)	
7	U 10/7	**Variable Declaration**: DW, DD. Offset and PTR operators. Constant declaration using EQU. DUP operator. **Input/Output using INT 21H**. Reading character, displaying character, displaying a string.	Chapter 3 & Section 12.5 (Assembly)	
	M 11/7			Input/Output
8	M 11/7	Input/Output using INT 21H.: Reading character, Displaying character, Displaying a string, Reading a string. Loop Instruction.	Chapter 3 & Section 12.5 (Assembly)	
9	T 12/7	**8086 registers**. **Memory Segmentation**, Logical & Physical Address. **(Quiz#2)**	Chapter 3 & 5 (Assembly)	
	S 16/7			Segment. & Addressing Modes
10	S 16/7	**8086 Addressing Modes**: Immediate, Register, Direct, Register-Indirect, Based, Indexed, Based-Indexed.	Chapter 3 & 5 (Assembly)	
11	U 17/7	**Pentium Registers**. **Pentium Addressing Modes**. Status & Flags Register.	Chapter 3 & 5 (Assembly)	
	M 18/7			Array indexing & Pentium Address. Modes
12	M 18/7	**Basic Pentium Instructions**: MOV, XCHG, LEA, MOVZX, MOVSX, BSWAP, XLATB. **(Quiz#3)**	Chapter 3 & 5 & 6 (Assembly)	
13	T 19/7	Basic Pentium Instructions: ADD, SUB, INC, DEC, NEG, ADC, SBB, CMP. Introduction to flow control instructions.	Chapter 3 & 5 & 6 (Assembly)	
	S 23/7			Arithmetic Instructions
14	S 23/7	**Multiplication Instructions**: MUL, IMUL. Pentium IMUL instructions. **Division Instructions**: DIV, IDIV. Sign Extension Instructions: CBW, CWD, CDQ, CWDE.	Chapter 6 & 3 (Assembly)	
15	U 24/7	Applications of Multiplication & Division instruction. Logical Instructions: NOT, AND, OR, XOR, Test. Applications of logic instructions. **(Solution of ExamI).**	Chapter 3 & 6 & 8 (Assembly)	
	M 25/7			Logical & Bitwise Instructions

16	M 25/7	**Shift Instructions**: SHL, SAL, SHR, SAR. Applications of using shift instructions in performing multiplication. Applications of using shift instructions in performing division. SHLD, SHRD.	Chapter 3 & 6 & 8 (Assembly)	
17	T 26/7	**Rotate Instructions**: ROL, ROR, RCL, RCR. Applications of rotate instructions. **(Quiz#4)**	Chapter 3 & 6 & 8 (Assembly)	
	S 30/7			Flow Control Instructions
18	S 30/7	**Flow Control Instructions**: Unconditional JMP. Types of jump target: Short, Near, Far. Conditional Jump instructions: Signed and Unsigned. Single-flag jump instructions. Loop Instructions: Loop, Loope/Loopz, Loopne/Loopnz. High-Level Decision Control Structures: IF-Then-Else, For Loop, Case.	Chapter 7 & 4 (Assembly)	
19	U 31/7	Case, While Loop, Repeat Until. Indirect Jump Example. **The Stack**: PUSH and POP instructions, PUSHA, POPA, PUSHAD, POPAD, PUSHF, POPF, PUSHFD, POPFD**. Introduction to Procedures**: CALL and RET.	Chapter 7 & 4 (Assembly)	
	M 1/8			Procedures & Macros
20	M 1/8	Procedure Definition, Near and Far Procedures, RET n instruction. Passing Parameters to Procedures. Examples of Procedures. **(Quiz#5)**	Chapter 7 & 4 (Assembly)	
21	T 2/8	**Introduction to Macros**. Macro Definition & Expansion. Pseudo parameters in macros. Macros versus procedures. Macro Library. Examples of Macros. REP and IRP macros. Conditional assembly. List Control Directives.	Chapter 10 (Assembly)	
	S 6/8			String Instructions
22	S 6/8	**String Instructions**: MOVS, MOVSB, MOVSW, MOVSD. REP Prefix. CMPS, CMPSB, CMPSW, CMPSD, SCAS, SCASB, SCASW, SCASD, LODS, LODSB, LODSW, LODSD, STOS, STOSB, STOSW, STOSD, REPE, REPNE. Applications of string instructions.	Chapter 9 (Assembly)	

23	U 7/8	**Input/Output**: IN and OUT instructions, Direct and Indirect I/O. **Introduction to Interrupts**. Difference between interrupts and procedures. Types of Interrupts: Hardware. Software, Exceptions. Maskable and non-maskable Interrupts, Interrupt Flag. **(Quiz#6)**	Chapter 12 (Assembly)	
	M 8/8			Interrupts
24	M 8/8	IVT, Interrupt Processing, Bios and DOS interrupts. **CPU Design**: Control unit and Data Path. Register Transfer. **Data-Path Design**. Connecting Registers using Muxs. Connecting Registers using a tri-state bus. Examples of register transfer: MOV, XCHG, ADD.	Chapter 12 (Assembly) Chapter 2 & 4 (Organization)	
25	T 9/8	Register Transfer Timing: Estimating Minimum Clock Period. **Single-Bus CPU Data path design**. Single-Bus CPU design: Fetch Control Sequence, Synchronous vs. Asynchronous Memory Transfer, Execution Control Sequence for MOV, ADD, XCHG, INC, ADD with register indirect addressing mode, unconditional Jump.	Chapter 2 & 4 (Organization)	
	S 13/8			Video Memory
26	S 13/8	Execution Control Sequence for conditional Jump, CMP, and LOOP. Performance Considerations. **Two-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD with register indirect addressing mode, unconditional and conditional Jump. **Three-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD, unconditional and conditional Jump Instructions.	Chapter 2 & 4 (Organization)	
27	U 14/8	**Control Unit Design: Hardwired Control Unit**, General Hardwired Control Unit Organization, Generation of Control Signals. Solution of Exam II.	Chapter 4 (Organization)	
	M 15/8			Using the Mouse
28	M 15/8	Deriving Rout & Rin Signals. CPU-Memory Interface Circuit.	Chapter 4 (Organization)	
29	T 16/8	***Microprogrammed Control Unit Design:*** Control Word, Control Store, Microinstruction, Microroutine. General	Chapter 2 & 4 (Organization)	

		Organization of Microprogrammed Control Unit, Micro Program Counter, Micro Instruction Register. Sequencer, Branching Address. Horizontal, Vertical and Field-encoded control store.		
	S 20/8			Serial Port
30	S 20/8	Vertical control store. Microroutine for Add instruction with 8 addressing modes. Wide branch addressing and Multiway branching. Bit Oring. Comparison of Hardwired vs. Microprogrammed control unit.	Chapter 2 & 4 (Organization)	
31	U 21/8	Simple CPU Design Example. Review.		
32	M 22/8	No Class.		