KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 062 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	S 17/2	Syllabus. Introduction, Assembly and machine language, Compiler and assembler.	Chapter1 & Int. Computer Org. & Assembly Lang. Prog. (Online)
2	M 19/2	Instruction and machine language, Instruction fields: opcode, operands, Assembly vs. Machine code, Translating languages, Advantages of High-Level languages, Why learn Assembly language, Assembly vs. High-level languages.	Chapter1 & Int. Computer Org. & Assembly Lang. Prog. (Online)
3	W 21/2	Assembly language programming tools: Assembler, Linker, Debugger, Editor. Programmer's view of a computer system. Instruction set architecture, Main components of a computer system.	Chapter1 & Int. Computer Org. & Assembly Lang. Prog. (Online)
4	S 24/2	Data Representation: Binary Numbers, Hexadecimal Numbers, Base Conversions, Integer Storage Sizes, Binary and, Hexadecimal Addition, Signed Integers.	Chapter1 & Data Representation (Online)
5	M 26/2	Two's complement representation, Sign extension, 16's complement, binary and hexadecimal subtraction, Ranges of signed integers, carry and overflow.	Chapter1 & Data Representation (Online)
6	W 28/2	Character representation: ASCII code, parity bit. IA-32 Architecture: Basic computer organization, processor, clock, memory, ROM and RAM.	Chapter1 & Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online)
7	S 3/3	Memory Hierarchy: Registers, RAM, Cache, Hard disk. **(Quiz#1)**	Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online)
8	M 5/3	Magnetic Disk Storage access time, Intel Microprocessors: History of processors. CISC vs. RISC processors.	Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online)
9	W 7/3	IA-32 Registers, Status Flags, Fetch-Execute cycle.	Chapter 2 & Int. Computer Org. and

			Assembly Lang. Prog. (Online)
10	S 10/3	Pipelined Execution, Superscalar Architecture, IA-32 Memory Management, Modes of Operation, Real Address Mode: Logical to Linear Address Translation.	Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online)
11	M 12/3	Flat Memory Model, Protected Mode Architecture and address translation, Segment Descriptor Tables, Paging. Basic Elements of Assembly Language, Flat Memory Program Template, Assembling, Linking, and Debugging Programs.	Chapter 2 & 3 Assembly Language Syntax and Program Structure (Online)
12	W 14/3	**Variable Declaration**: DB, BYTE, SBYTE. Defining strings. DUP Operator.	Chapter 3 & Variable, Constant, and Array Declaration (Online)
13	S 17/3	Variable Declaration: DW, WORD, SWORD, DD, DWORD, SDWORD, Byte Ordering, Defining Symbolic Constants: =. **(Quiz#2)**	Chapter 3 & Variable, Constant, and Array Declaration (Online)
14	M 19/3	Defining Symbolic Constants: EQU & TEXTEQU Directives. Offset Operator, Align Directive, Type, Lengthof, Sizeof operators.	Chapter 3 & Variable, Constant, and Array Declaration (Online)
15	W 21/3	PTR operator, Label directive. Operand Types.	Chapter 3 & Variable, Constant, and Array Declaration (Online)
16	S 24/3	**Basic Pentium Instructions**: MOV, XCHG. MOVZX, MOVSX, ADD, SUB.	Chapter 4 (Assembly) Basic Pentium Instructions (Online)
17	M 26/3	ADD, SUB, INC, DEC, NEG, ADC, SBB.	Chapter 4 (Assembly) Unit4: Basic Pentium Instructions (Online)
18	W 28/3	JMP & Loop Instruction. Addressing Modes: Immediate, Register, Direct, Register Indirect.	Chapter 4 (Assembly) &Addressing Modes (Online)
	Th 29/3	**MAJOR EXAM I**	
19	S 31/3	Indexed Addressing Mode. **(Solution of EXAM I).**	Chapter 4 (Assembly) &Addressing Modes (Online)

20	M 2/4	Addressing modes: Based, Indexed, Based-Indexed. 8086 Addressing modes. Two-dimensional array processing.	Chapter 4 (Assembly) &Addressing Modes (Online)
21	W 4/4	LEA instruction. Default segments and Segment Override. PC relative addressing.	Chapter 4 (Assembly) &Addressing Modes (Online)
22	S 7/4	Link Library Overview, Calling a Library Procedure, Linking to a Library, Input/Output procedures using book's library (Irvine32.lib).	Chapter5 (Assembly)
23	M 9/4	Input/Output libraries, **Stack instructions**: Push and Pop.	Chapter5 (Assembly) & Stack & Procedures (Online)
24	W 11/4	Uses of the Runtime Stack: Temporary Storage of Registers, Nested Loop, Saving Return Address, Local Variable Declaration. **(Quiz#3)**	Chapter5 (Assembly) & Stack & Procedures (Online)
25	M 16/4	Stack Instructions: pushad, pusha, popad, popa, pushfd, pushf, popfd, popf. **Defining and Using Procedures**, Call & RET Instructions, Parameter Passing, Preserving Registers, USES Operator, Program Design using Procedures.	Chapter5 (Assembly) & Stack & Procedures (Online)
26	W 18/4	Program Design using Procedures, Parameter Passing Through Stack, Call & Return Instructions, Freeing Passed Parameters From Stack, Local Variables.	Chapter5 (Assembly) & Stack & Procedures (Online)
27	S 21/4	**Logical Instructions**: NOT, AND, OR, XOR, Test, NOT. Applications of logic instructions. **Flow Control Instructions**: CMP Instruction. Conditional Jump instructions: Unsigned.	Chapter6 (Assembly) & Flow Control Instructions (Online)
28	M 23/4	Conditional Jump instructions: Signed and Unsigned. Single-flag jump instructions.	Chapter6 (Assembly) & Flow Control Instructions (Online)
29	W 25/4	Conditional Loop Instructions: Loope/Loopz, Loopne/Loopnz. **(Quiz#4)**	Chapter6 (Assembly) & Flow Control Instructions (Online)
30	S 28/4	Conditional Loop Instructions: Loope/Loopz, Loopne/Loopnz. High-Level	Chapter6

		Decision Control Structures: IF-Then-Else, For Loop, Case. While Loop.	(Assembly) & Flow Control Instructions (Online)
31	M 30/4	Indirect Jump and Table-Driven Selection, case statements, bubble sort.	Chapter6 (Assembly) & Flow Control Instructions (Online)
32	W 2/5	**Shift Instructions**: SHL, SAL, SHR, SAR. Applications of using shift instructions in performing multiplication. Applications of using shift instructions in performing division. SHLD, SHRD. **Rotate Instructions**: ROL, ROR, RCL, RCR.	Chapter7 (Assembly) & Bit Manipulation Instructions (Online)
33	S 5/5	Shift & Rotate Applications. **Multiplication Instructions**: MUL, IMUL. Pentium IMUL instructions.	Chapter7 (Assembly) & Advanced Arithmetic (Online)
	S 5/5 Makeup	**Division Instructions**: DIV, IDIV. Sign Extension Instructions: CBW, CWD, CDQ. Translating Arithmetic Expressions, Decimal string to number conversions.	Chapter7 (Assembly) & Advanced Arithmetic (Online)
34	M7/5	Number to decimal string conversion. **String Instructions**: MOVS, MOVSB, MOVSW, MOVSD. REP Prefix. CMPS, CMPSB, CMPSW, CMPSD. SCAS, SCASB, SCASW, SCASD, LODS, LODSB, LODSW, LODSD, STOS, STOSB, STOSW, STOSD, REPE, REPNE. Applications of string instructions.	String Handling Instructions (Online)
35	W 9/5	**Input/Output**: IN and OUT instructions, Direct and Indirect I/O. **Introduction to Interrupts**. Difference between interrupts and procedures. Types of Interrupts: Hardware. Software, Exceptions. Maskable and non-maskable Interrupts, Interrupt Flag. Interrupt Processing, IVT, Trap Flag.	Input/Output Instructions & Interrupts (Online)
36	S 12/5	Review of Interrupt processing. **(Quiz#5)**	Input/Output Instructions & Interrupts (Online)
37	M 14/5	**CPU Design**: Register Transfer. **Data-Path Design**. Connecting Registers using Muxs.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)

	M 14/5	MAJOR EXAM II	
38	W 16/5	Connecting Registers using a tri-state bus. Examples of register transfer: MOV, ADD, SUB, INC.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
39	S 19/5	Examples of register transfer: INC, DEC, XCHG. . **Register Transfer Timing**: Estimating Minimum Clock Period. **Single-Bus CPU Data path design**: Fetch Control Sequence.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
40	M21/5	**Single-Bus CPU**: Synchronous vs. Asynchronous Memory Transfer, Execution control sequence for ADD with register indirect addressing mode, unconditional & Conditional JMP, Add with immediate.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
41	W 23/5	**Single-Bus CPU**: Execution control sequence for Conditional JMP, INC, Loop, CMP instructions. Performance Considerations. **Two-Bus CPU**: Fetch Control Sequence.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
42	S 26/5	**Two-Bus CPU**: Execution Control Sequence for ADD with register indirect addressing mode, unconditional and conditional Jump. **Three-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD, unconditional and conditional Jump Instructions. **Control Unit Design: Hardwired Control Unit.**	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
43	M28/5	**Hardwired Control Unit**, General Hardwired Control Unit Organization, Generation of Control Signals. Deriving Rout & Rin Signals. **CPU-Memory Interface Circuit.**	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
44	W 30/5	**CPU-Memory Interface Circuit. Microprogrammed Control Unit Design*:*** Control Word, Control Store, Micro Program Counter, Micro Instruction Register, Microinstruction, Microroutine.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
45	S2/6	General Organization of Micro-programmed Control Unit, Branching Address, Sequencer. Horizontal, Field-encoded and vertical control store. Comparison of Hardwired vs. Micro-programmed control unit.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)