

Jan. 26, 2007

COMPUTER ENGINEERING DEPARTMENT

COE 205

COMPUTER ORGANIZATION & ASSEMBLY PROGRAMMING

Final Exam

First Semester (071)

Time: 7:00 -9:30 PM

Student Name : __KEY_____

Student ID. : _____

Question	Max Points	Score
Q1	12	
Q2	28	
Q3	40	
Q4	20	
Total	100	

Dr. Aiman El-Maleh

[12 Points]

(Q1) A typical PC system today has: 3 GHZ Pentium IV Processor, 256-1024 Mbytes main memory, 512-1024 Kbytes cache memory, hard disk with 10ms average access time and 10 Mbytes/sec transfer rate, and a CD-ROM drive. The Pentium IV processor is a 32-bit processor, has a 36-bit address bus, and a 64-bit data bus. Assume that the main memory is asynchronous and that it is byte-addressable.

- (i) Determine the maximum size of main memory that can be accessed by the Pentium IV processor. Give your answer in Mbytes or Gbytes.

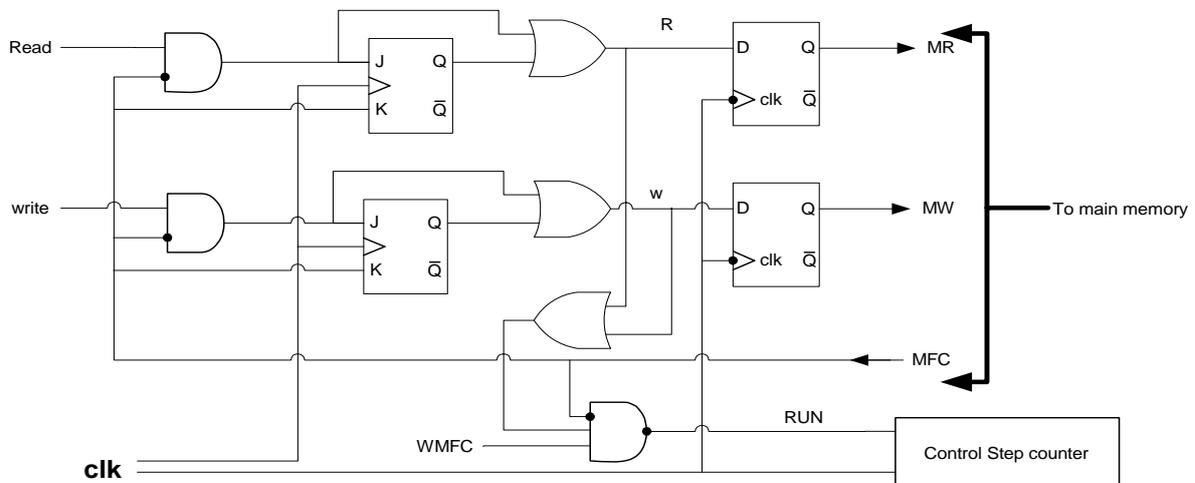
Address bus = 36 bits
 \Rightarrow maximum size of accessed memory is $2^{36} = 64$ GByte

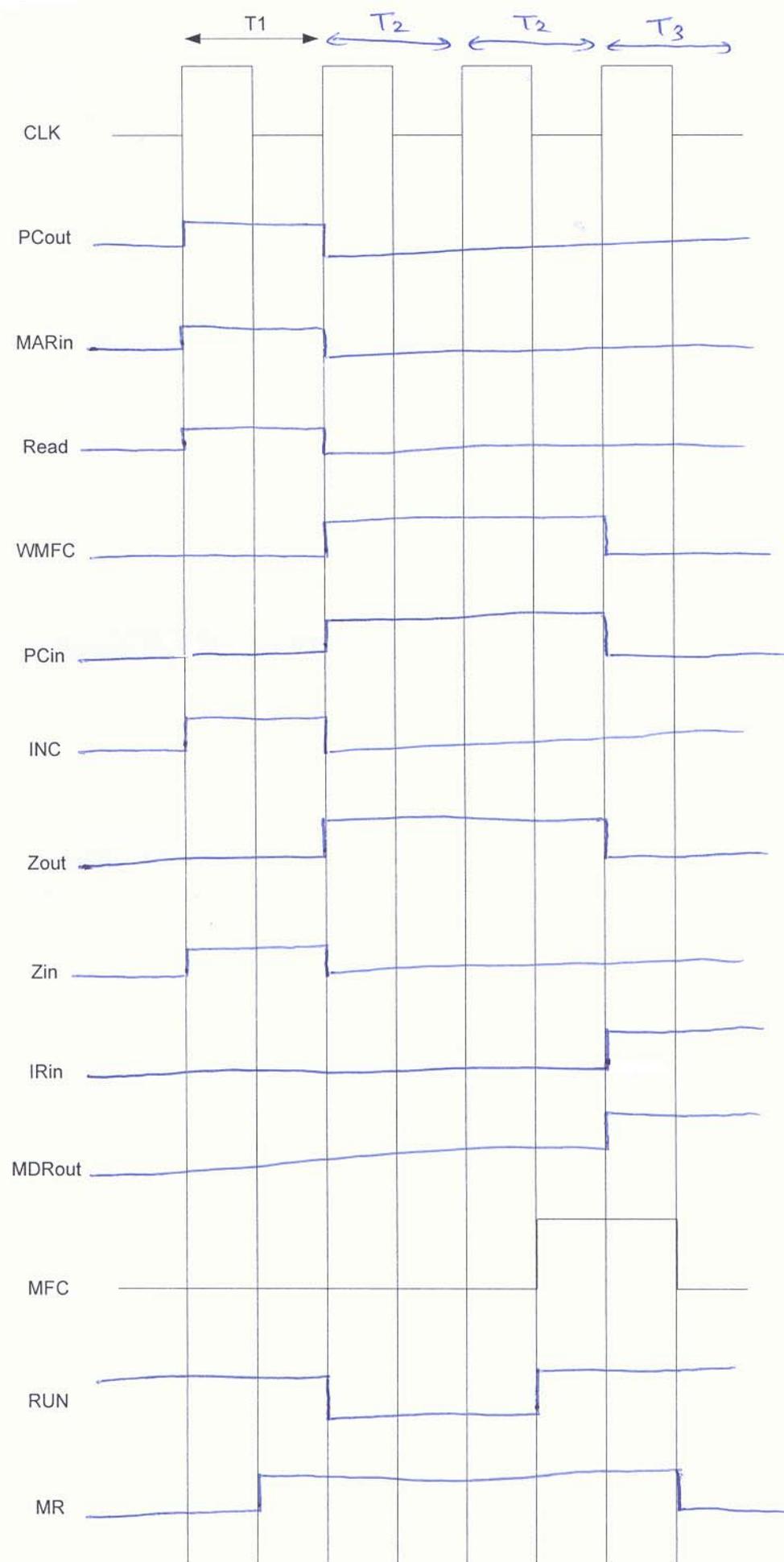
- (ii) What is the maximum number of bytes that can be transferred between the Pentium IV CPU and memory in a read or write cycle.

8 bytes since the data bus size is 64 bits.

- (iii) Given the CPU-Memory interface circuit shown below, complete the given timing diagram assuming the following fetch control sequence as shown below:

- T1 PCout, MARin, Read, INC, Zin
- T2 Zout, PCin, WMFC
- T3 MDRout, IRin

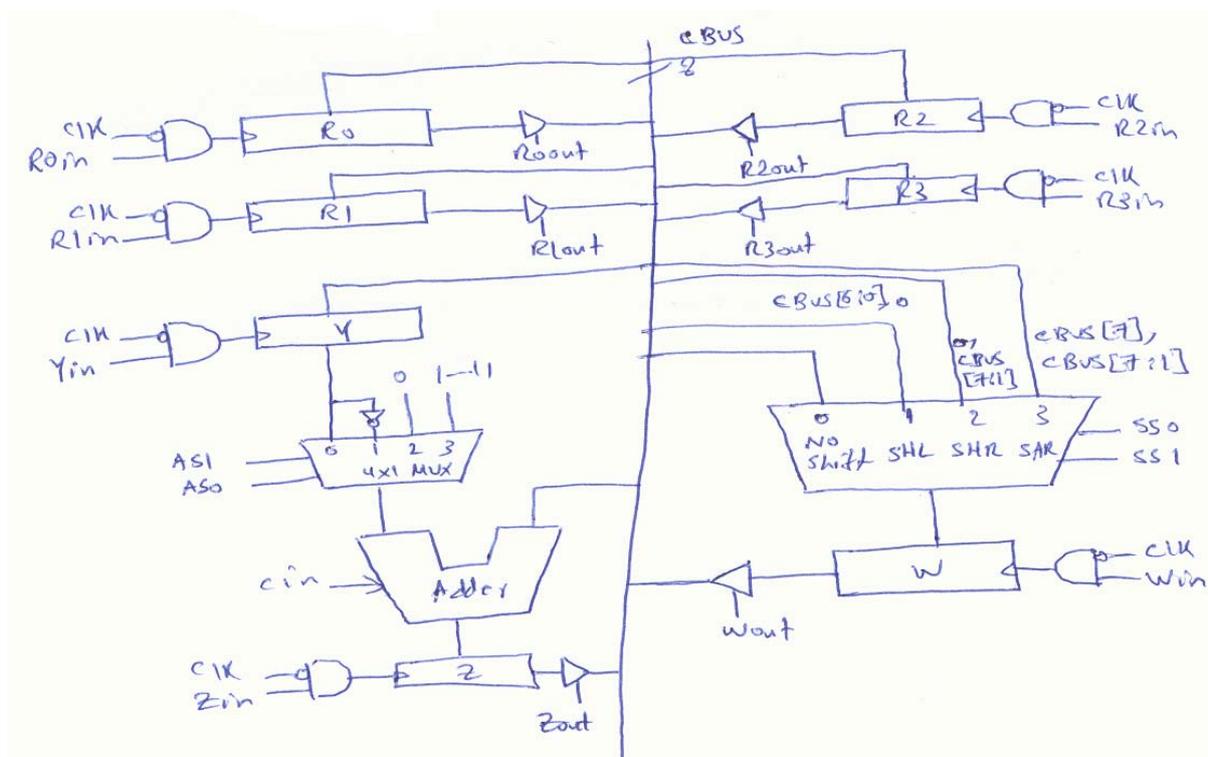




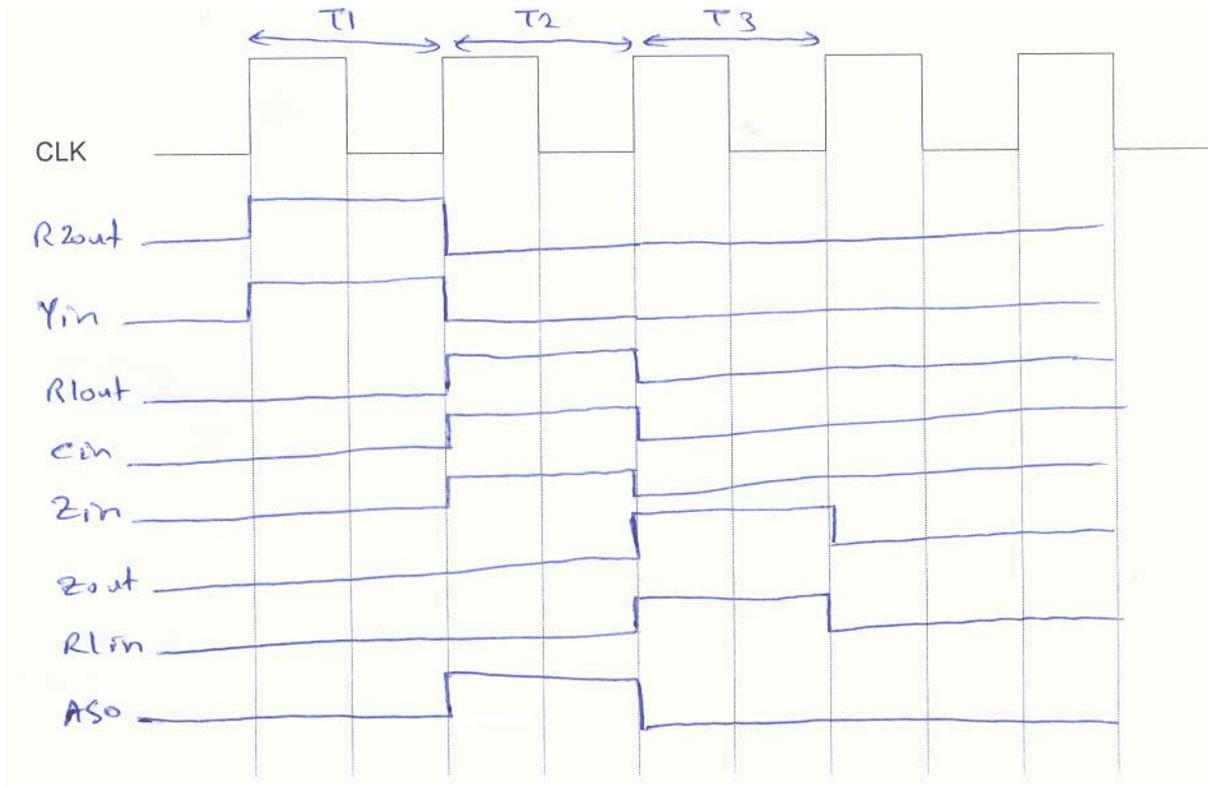
[28 Points]

(Q2) It is required to design a **data path** that has **four** 8-bit registers, namely R0, R1, R2, and R3. The data path should be able to do the following:

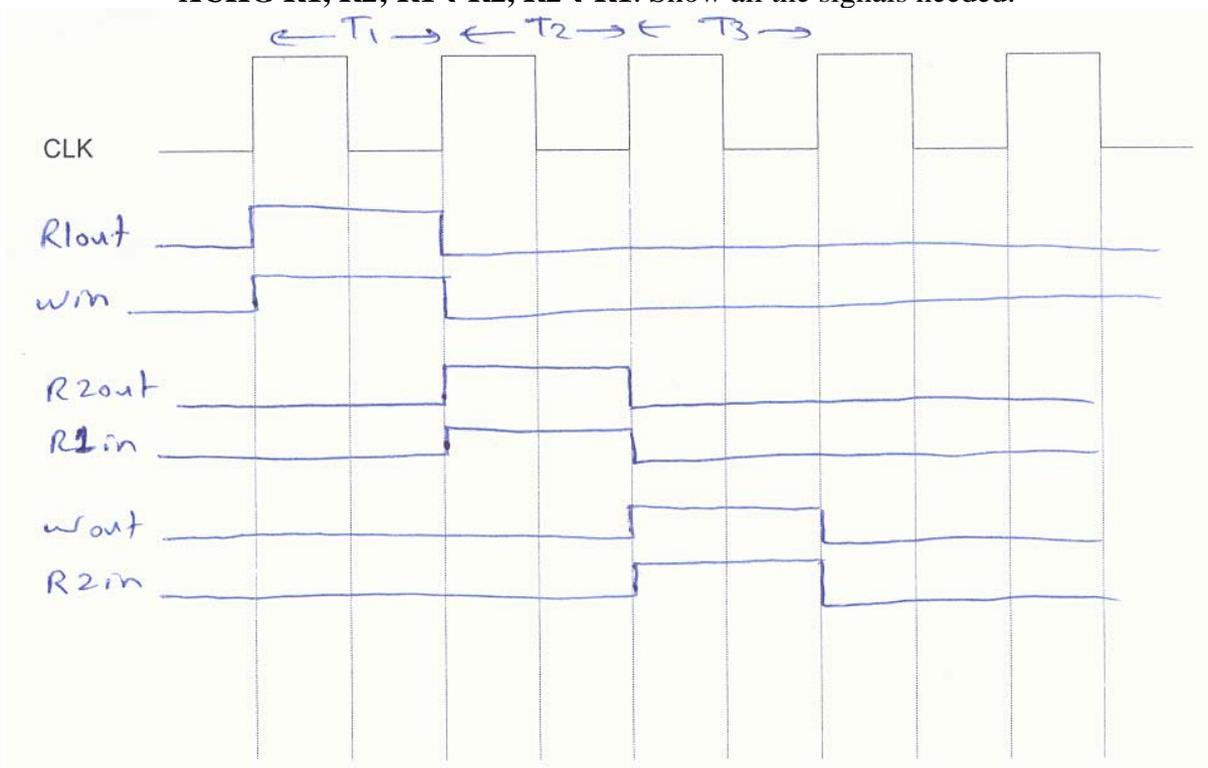
- **Move** the content of any register to any other register.
 - **Exchange** the content of any two registers.
 - **Add** the contents of any two registers and store the result in a destination register.
 - **Subtract** the contents of any two registers and store the result in a destination register.
 - **Increment** the content of a register by 1.
 - **Decrement** the content of a register by 1.
 - **SHL (Shift left), SHR (Shift Right) or SAR (Shift Arithmetic Right)** the content of a register by **1 bit** and store the result in the register itself.
- (i) Show the **data path logic design** using a **single tri-state bus**. Clearly illustrate all the design details and all the required control signals. Show clearly how each of these operations will be performed by the datapath. **Assume that you can only use the following type of combinational logic blocks: Adder, Inverter, AND, OR, XOR, Multiplexor, Tri-state buffer.** The adder can only do **addition** of its two inputs and a Carry-in signal. Note that you do not need to include the PC, IR, MAR, and MDR registers. **Design the data path to minimize the number of clock cycles needed for the execution of the specified instructions.**



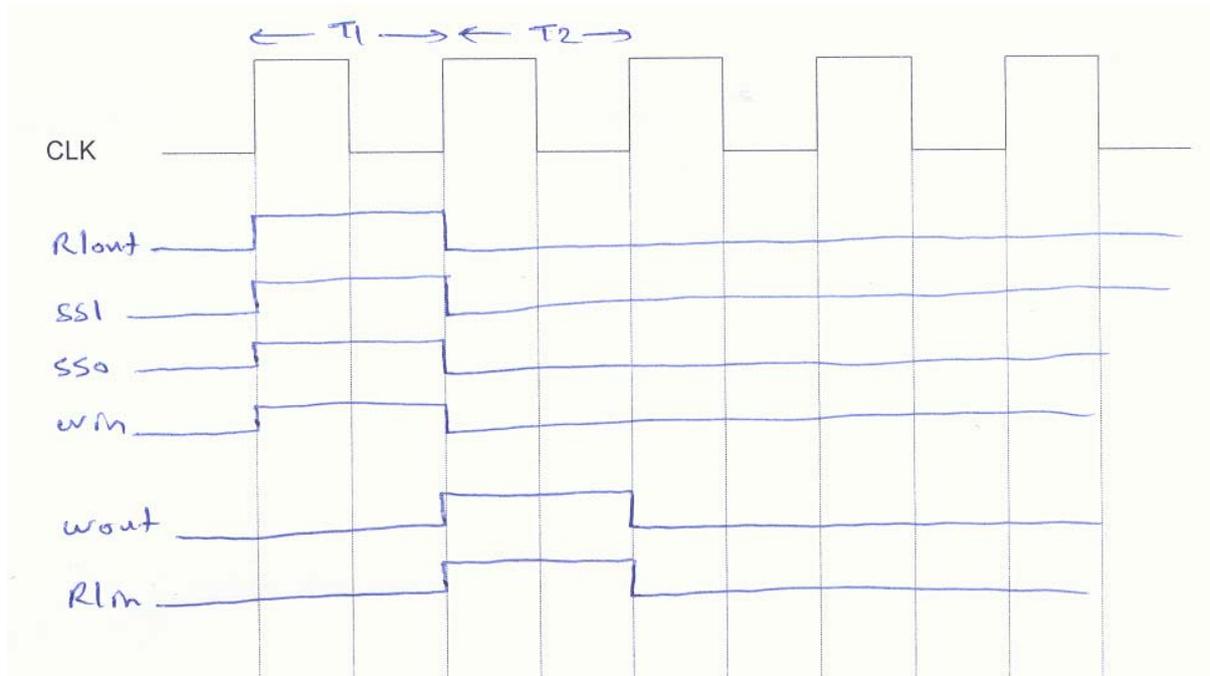
- (ii) Show the timing diagram for the execution control sequence of the operation **SUB R1, R2; R1 ← R1 - R2**. Show all the signals needed.



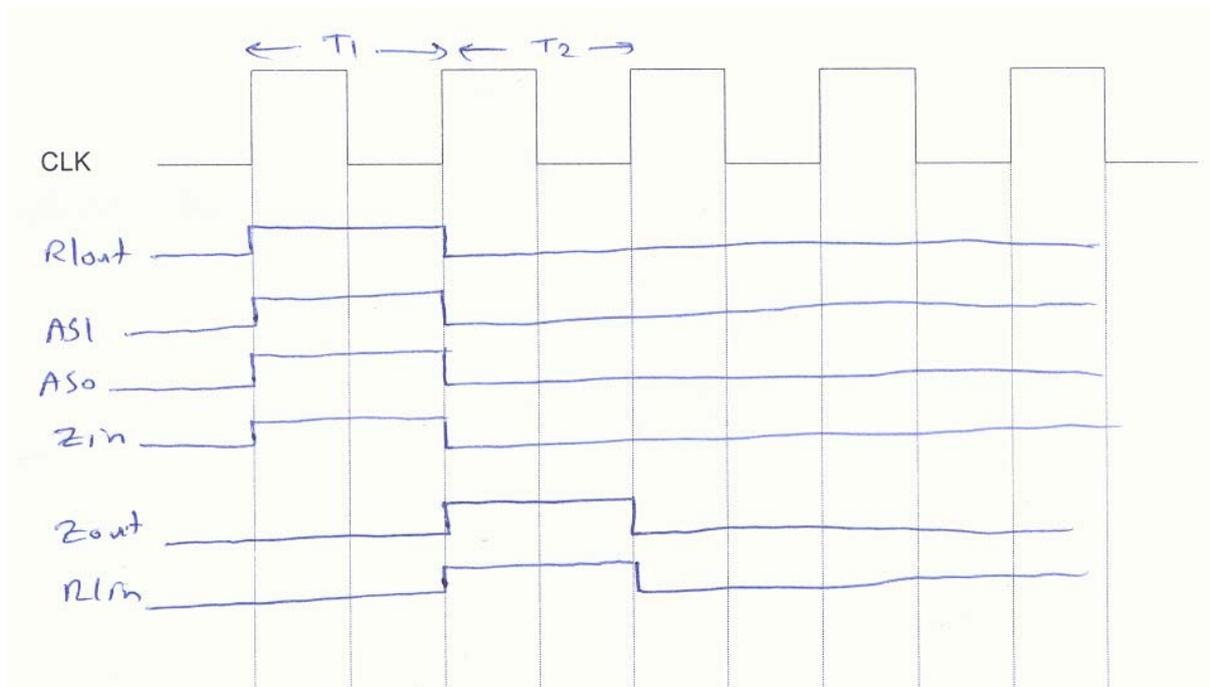
- (iii) Show the timing diagram for the execution control sequence of the operation **XCHG R1, R2; R1 ← R2, R2 ← R1**. Show all the signals needed.



- (iv) Show the timing diagram for the execution control sequence of the operation **SAR R1; Shift Arithmetic Right R1 by 1 bit**. Show all the signals needed.



- (v) Show the timing diagram for the execution control sequence of the operation **DEC R1; R1 ← R1 - 1**. Show all the signals needed.



[40 Points]

(Q3) Assume that a CPU has **16 instructions** with an opcode of 4 bits, seven **16-bit** general purpose registers namely AX, BX, CX, DX, SI, DI and SP, a **16-bit data bus**, and a **16-bit address bus**. Assume that all the instructions are 16-bit. The CPU has an **Arithmetic and Logic Unit (ALU)** with inputs A and B and output C, that can perform any of the following functions shown below based on the three selection lines AS2, AS1, and AS0:

AS2 AS1 AS0	Operation
000	$C=A+B$
001	$C=A-B$
010	$C=A+1$
011	$C=A-1$
100	$C=B$
101	$C=A+2$
110	$C=A-2$
111	$C=NOT A$

The CPU has also a **Shift Unit** that can perform shifting as shown below based on the two selection lines SS1 and SS0:

SS1 SS0	Operation
00	No shift
01	W=Shift logic right(X) by M bits
10	W=Shift logic left(X) by M bits
11	W=Shift arithmetic right(X) by M bits

Assume that the IR, PC, MAR, and MDR registers are also **16-bit registers**. Also assume that the instructions for this processor follow the syntax and semantics and addressing modes of the 8086 processor. Also assume that registers play the same role as assumed in the 8086 processor.

Assume that the data path of this processor is implemented using a **three-bus architecture** as shown in the next page.

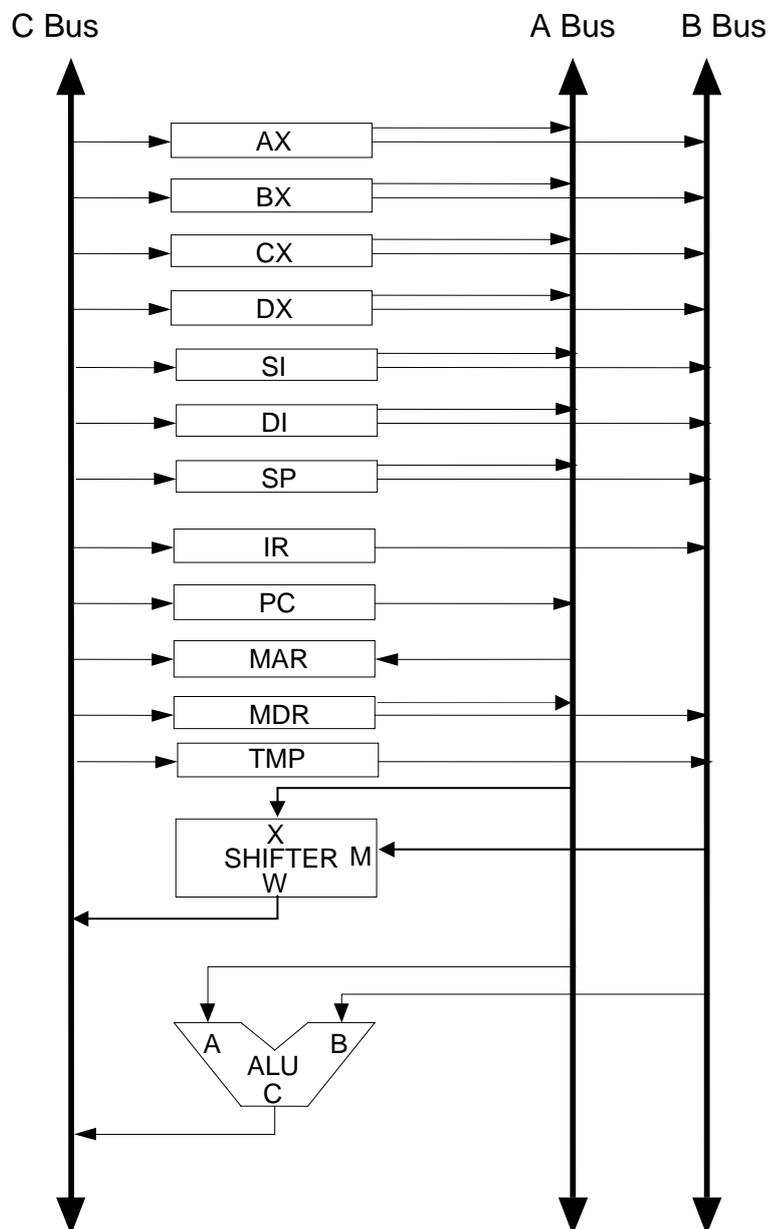
- (i) Determine the **maximum speed** at which this design will work given the following delay parameters:

Name	Parameter	Delay
Tri-state buffer propagation time	t_q	150 ps
Bus propagation time (assumed)	t_{bp}	500 ps
ALU delay	t_{ALU}	400 ps
Shifter delay	$t_{shifter}$	200 ps
Flip-flop propagation time	t_{ff}	440 ps
Flip-flop setup time	t_{su}	146 ps
Flip-flop hold time	t_h	104 ps

The clock period should be greater than the longest delay in the datapath

$$\Rightarrow T \geq t_g + 2 \cdot t_{bp} + t_{ALU} + t_{su} + t_{eff} = 2136 \text{ ps}$$

$$\Rightarrow F = \frac{1}{T} \leq \frac{1}{2136 \text{ ps}} = 468 \text{ MHz}$$



Data Path Design

- (ii) Write the minimum number of control steps required for fetching an instruction from memory.

T₁ PC_{out}, MAR_{in}, A, AS₂, AS₀ ALU (C=A+2)
 ALU_{out}, PC_{in}, Read, WMFC

T₂ MDR_{out}, B, AS₂ ALU (C=B), ALU_{out},
 IR_{in}

- (iii) Write the minimum number of control steps required for the execution of each of the following instructions:

- a. **SUB AX, 10** ; (Subtract the constant 10 from the content of register AX).

T₃ AX_{out}, A, IR_{out}, AS₀ ALU (C=A-B),
 ALU_{out}, AX_{in}, End

- b. **MOV AX, [BX]** ; (Move the content of the memory operand pointed by register BX into register AX).

T₃ BX_{out}, A, MAR_{in}, A, Read, WMFC

T₄ MDR_{out}, B, AS₂ ALU (C=B), ALU_{out},
 AX_{in}, End

- c. **INC ARRAY** ; (Increment the content of the memory operand ARRAY).

T₃ IR_{out}, AS₂ ALU (C=B), ALU_{out},
 MAR_{in}, c, Read, WMFC

T₄ MDR_{out}, A, AS₁ ALU (C=A+1), ALU_{out},
 MDR_{in},

T₅ write, WMFC

T₆ End

d. **PUSH AX** ; (Push the content of register AX on the stack).

T₃ SP_{out}, A, AS₂, AS₁ ALU (C=A-2),
 ALU_{out}, SP_{in}, MAR_{in}, C
 T₄ AX_{out}, B, AS₂ ALU (C=B), ALU_{out},
 MDR_{in}, write, WMFC
 T₅ End

e. **MOVSB** ; (move a byte from the memory address pointed by SI into the memory address pointed by DI and increment both SI and DI by 1).

T₃ SI_{out}, A, MAR_{in}, A, AS₁ ALU (C=A+1),
 ALU_{out}, SI_{in}, Read, WMFC
 T₄ DI_{out}, A, MAR_{in}, A, AS₁ ALU (C=A+1),
 DI_{in}, ALU_{out}
 T₅ write, WMFC
 T₆ End

f. **JE label** ; (Jump to the address label if the zero flag is 1).

T₃ IR_{out}, PC_{out}, ALU (C=A+B), ALU_{out}
 if (ZF=1) PC_{in}, End

- g. **SAR SI, 5** ; Shift arithmetic right register SI by 5 bit.

T_3 IRout, STout, A, SSI, SSO SAR(w, M)
Wout, STin, End

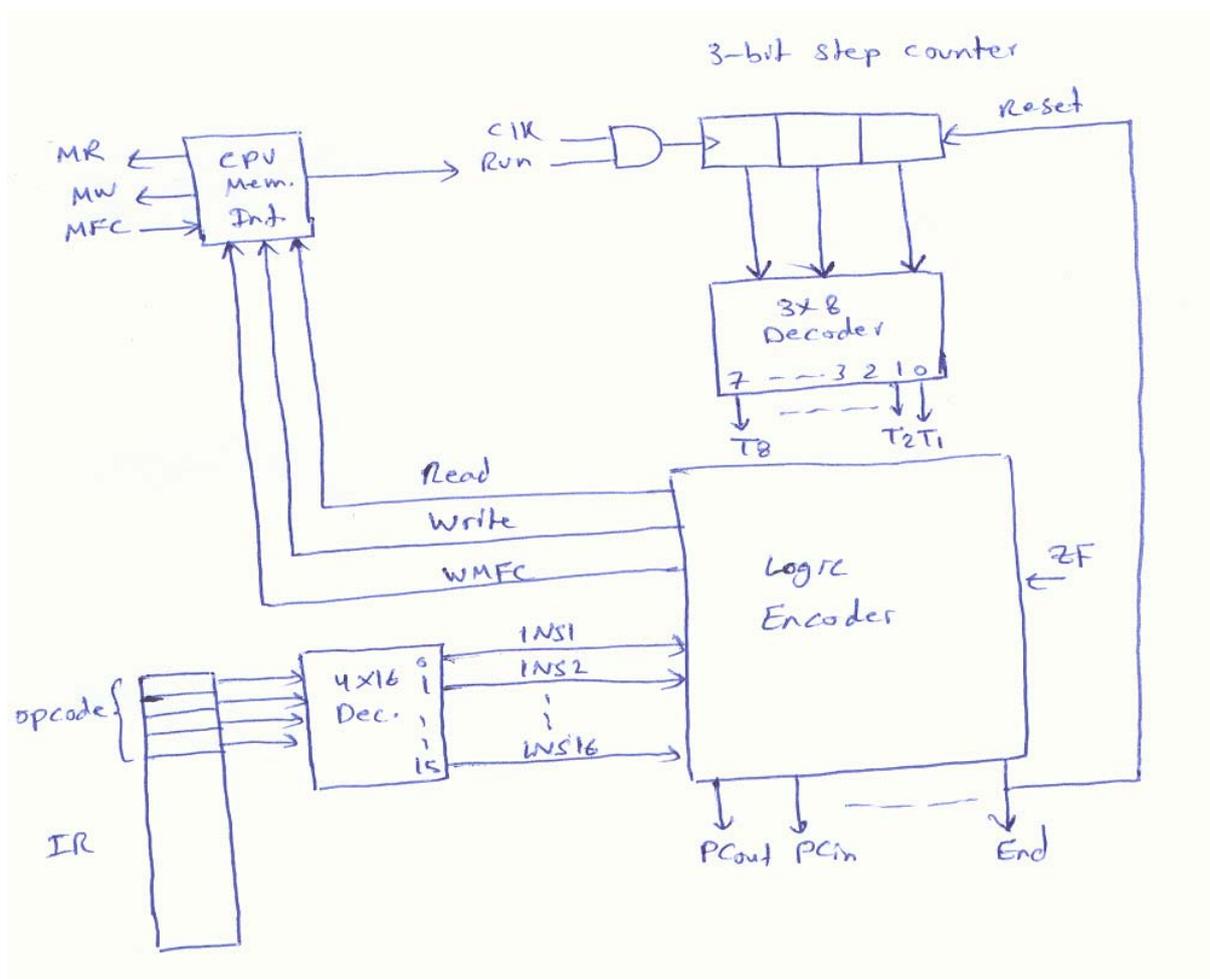
- (iv) Based on the fetch and execution control sequence of the seven instructions given in this question, show the logic equation required for generating the signal **PCin**.

$$PCin = T_1 + JE \cdot ZF \cdot T_3$$

[20 Points]

(Q4) Using the CPU described in the previous question and the given data path, it is required to implement the control unit for this CPU using both hardwired and microprogrammed approach. Assume that the number of signals that have to be generated by the control unit to control the data path and the memory interface circuit for this CPU is 40 signals.

- (i) Assume that the maximum number of control steps required for the fetch and execution of any of the 16 instructions is 8 control steps. Show the block diagram of the **hardwired control unit** organization for this CPU indicating all the necessary components and signals. Clearly indicate the size of the various components.



- (ii) Assume that the control unit for this CPU is to be implemented using a microprogrammed approach and that the number of different control words to be stored in the control store for all the microroutines is **60 CWs**. Also, assume that the microprogrammed control unit design should support unconditional branch (UBR), branch on zero (BRZ), branch on negative (BRN), branch on carry (BRC).

- a. Show the format and size of the control word using **horizontal control store**. What is the size of the control store needed?

Since the number of control words = 60,
 the μ Branch address = 6 bits
CW Format:
 MS1, MS0, UBR, BRZ, BRN, BRC, 40 bits
 for the control signals, 6 bits for μ Branch
 address = 52 bits.
 Size of control store = 60 x 52 bits

- b. Show the block diagram of the **microprogrammed control unit** organization for this CPU indicating all the necessary components and signals. Clearly indicate the size of the various components.

