COE 203 Digital Logic Laboratory
Development Proposal
One-Month Summer Assignment (Term 063)
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1. Introduction

The digital logic laboratory course is taken by computer engineering, computer science and software engineering students following the COE 202 course titled: "Digital Logic Design". The COE 203 course consists of a set of laboratory experiments for students to gain hands-on experience in digital logic. It also emphasizes the use of state-of-the-art CAD tools and boards for the design, simulation, and implementation of digital logic. Combinational and sequential digital systems as well as data and control path design experiments are conducted.

The learning outcomes of this course are:

Outcome 1: The ability to design combinational and sequential circuits to meet certain specifications **[ABET Criterion 3c]**
Outcome 2: The ability to use tools and discrete components, EEPROMs, FPGAs, to model, simulate and implement digital circuits. **[ABET Criterion 3k]**
Outcome 3: The ability to design and conduct experiments related to digital systems and to analyze their outcomes. [**ABET Criterion 3b**]
Outcome 4: The ability to work in teams. [**ABET Criterion 3d**]
Outcome 5: The ability to communicate effectively. [**ABET Criterion 3g**]

The existing structure of the lab manual is as follows:

Week#	Experiment
1	Review of combinational circuit design.
2	Review of sequential circuit design.
3	Experiment#1 Prototyping of Logic Circuits using Discrete Components: Full Adder
4	Experiment#2 Prototyping of Logic Circuits using EEPROMs: Sequence Detector
5	Experiment#3 Introduction to FPGA Design Flow: Full Adder
6	Experiment#4 Simple Traffic Light Controller
7	Experiment#5 Verilog Based Design of Ripple Carry Adder
8	Experiment#6 RTL Verilog Based Design of an Arithmetic Logic Unit
9	Experiment#7

	Finite State Machine Design in Verilog (Traffic Light Controller)
10 & 11	Experiment#8 Designing a Programmable Digital Lock
12-14	Project
15	Project Evaluation

2. Need of the Project

This course is a practical course based on design and implementation of digital systems. It is a good place to let students experience the design process and learn it in the proper way. Traditional teaching methods do not deliver design aspects in an effective way to maximize students' learning. Thus, design has to be injected following modern principles based on inductive learning approaches including project-based learning. It is demonstrated in the literature that project-based learning and need-based learning are more effective than traditional deductive learning approaches based on lecturing. In addition, as required by ABET, it became essential to revisit our courses to focus on the coverage of course outcomes, which map directly to ABET outcomes. Thus, it is apparent that design aspects have to be carefully injected starting from low level courses including COE 203.

Based on both initial students' feedback and feedback from faculty who taught the course and based on reviewing the lab manual, it is apparent that the lab needs improvements to better address the course learning outcomes. The current lab structure does not address well some of the learning outcomes and is mainly based on traditional teaching where students are taught how to do things and they are then asked to do similar things following a given procedure. In all the experiments, design is given to students and students are not given the chance to come up with the design themselves and explore different solutions.

Closely examining the lab manual, one can observe the following areas that certainly need improvement:

1. Coverage of Outcome 1 (design) needs enhancements. In all the experiments in the lab manual, the design is given to the students. Students should not be given the design and should be asked to think and come up with the design themselves. Then, their designs should be discussed by lab instructors and they should be guided to the correct solution. This will certainly improve their design abilities.
2. Outcome 3 is not well addressed in the lab and certainly needs more emphasis. There is no experiment given that requires the students to design an experiment themselves and decide what methodology they will use to collect data.
3. Some experiments may not need a whole dedicated week. For example, the experiments on the use of discrete components and EPROM may be merged together if carefully designed.
4. Three experiments are spent on teaching the students modeling using verilog. Teaching students HDL (Verilog) as a design entry is good but should not be the main objective of the experiments. Verilog modeling should be injected and integrated with many experiments where students will learn that through practice. The focus should be on

design. One week giving a verilog tutorial with hand on practice should be sufficient. Then, verilog will be injected and integrated with all following experiments.

5. The first two weeks are spent on the review of combinational and sequential circuit design. I think that one week is enough. Students will review these concepts on a need basis through doing the experiments. Need-based learning is more effective.
6. The lab manual organization and content needs improvement. All the experiments are described in a detailed step-by-step procedure. This style should be only followed in the first few experiments. Also, the description of experiments should be clear and well described. There is duplicate text between experiments. For example, the design specifications in Experiment 1 and Experiment 3 are an exact copy. The same applies for experiment 4 and Experiment 7. There are also some errors that need to be fixed. For example, the magnitude comparator is incorrectly designed as a tree of XOR gates. The traffic light controller is designed with four states while three are sufficient. Also the design given has problems with it!! In general, the style of preparing the experiments needs improvements.
7. Feedback from students indicates that this is a one-credit hour course and a lot of work outside the lab is requested from them in writing lab reports. Also, it was indicated that in several lab experiments they could not finish on time making the lab instructors extend the time (one hour extension in one case). Some lab instructors change the experiments but it does not seem to be serving the objectives of the experiment. This clearly indicates that the experiments have to be carefully designed with a clear objective with simplicity in mind.

3. Benefit

My plan in redesigning the experiments is to follow a project-based learning and need-based learning approach with a focus on achieving all course outcomes. The focus will be on designing a small number of experiments with each experiment having a clear objective to achieve. In addition, experiments will be designed to be enjoyable and simple at the same time. The intention is to redesign the lab around four main experiments. The advantage of this is that each experiment will span a period of 2-3 weeks. This allows better continuity and removes the burden on some students who could not finish certain parts on time. All experiments will be conducted based on a group of two students to inject teamwork. Top-down design methodology and bottom-up implementation methodology will be used. Having four main experiments implies that students have to write only four lab reports, which reduces their effort and makes their work more focused.

Also, a suggested approach is that students should not be allowed to move to the next experiment unless they complete the previous experiment. This will ensure that all students receive proper attention from their lab instructors and all have a successful learning experience. This will make the lab more dynamic allowing students to move at their own pace and removing the constraint of not being able to finish some of the experiments, forcing lab instructors to either change the experiment or cancel certain parts in it.

The proposed lab redesign is shown in the next table.

Week#	Experiment
1	Review of combinational & sequential circuit design.
2-3	**Experiment#1** **Main Objective: Introduce students to design and implementation using discrete components, EPROM and FPGAs.** Methodology: The design will be based on a simple serial adder that will be implemented using the three different approaches.
4	**Verilog Tutorial with Hands-On Experience** **Main Objective: Introduce students to modeling based on Hardware description language (Verilog)**. Methodology: Students will learn different modeling styles including structural, RTL and behavioral through simple examples including: serial adder, ripple carry adder, sequence detector, simple ALU.
5-6	**Experiment#2** **Main Objective: Practice Sequential Circuit Design Process.** Methodology: The students will be asked to design a traffic light controller with practical timing constraints. They will be asked to do the design process using schematic capture to go over the design process they learned in COE 202. Then, verilog based design will be given to them to appreciate the advantage of using HDL as a design entry.
7-8	**Experiment#3** **Main Objective: Introduce students to Datapath design and address the ability to design and conduct experiments and to analyze and interpret data.** Methodology: Students will be asked to design a simple single bus datapath interconnecting four registers and a simple ALU. They will be asked to analyze the maximum frequency across which their design will work. They will also be asked to suggest design changes to make the speed of their design faster. This involves changing the adder from ripple carry adder to carry–look ahead adder. They will conduct experiments to perform timing analysis of the two adders.
9-11	**Experiment#4** **Main Objective: Introduce students to Design Tradeoffs.** Methodology: Students will be asked to design a circuit with several possible design solutions that have different design tradeoffs. One suggestion is the design of a 4-bit multiplier under both area constraint and timing constraints. Students will be asked to come up with two different designs satisfying the given constraints.

12-14	**Project** Main Objective: The project will focus on a design problem that integrates datapath and control unit design, where the students will integrate the knowledge they have experienced through conducting the four experiments in coming up with an efficient solution meeting the given design requirements. The project will change from one semester to another.
15	Project Evaluation

The main benefits from this project can be summarized as follows:

- Better coverage and emphasis of course learning outcomes
- Early focus on design
- Enhancing student learning experience following modern learning techniques
- Improved lab manual

To maximize the benefit of this project, comments of students based on last and this semester will be collected. Also, all faculty involved in teaching this lab will be asked to provide their suggestions for lab improvement and the problems encountered. Feedback from faculty on the proposed lab development will be taken into account before the project starts. I also think that it will be a good idea that I teach the lab in the summer while working on the project to experience the actual lab setup and see the difficulties encountered. This will certainly help in improving the lab development.

The lab will be ready to be carried out starting 071. I will be willing to coordinate the lab during that semester and help lab instructors to guarantee a smooth transition.

4. Deliverables

By the end of this project, the following will be delivered:

1. A complete and well-organized lab manual.
2. Experiment solutions and all necessary lab files to be given to lab instructors.
3. Enhanced lab guide.
4. A PowerPoint Verilog tutorial to be used by lab instructors.
5. A list of suggested projects to be used by lab instructors.

All proposed experiments will be implemented and tested to avoid any unpredictable incidence.

5. Team & Duration

I think that one person working on this project should be sufficient. A one-month summer compensation is required for completing the proposed work. The work will span the whole two-months summer period and should be ready by the end of summer.