

Name: KEY

Id#

COE 202, Term 052
Fundamentals of Computer Engineering

Quiz# 4 (Take Home)

Due date: Monday, April 10, 2006

Q.1. You are required to design a circuit that computes the remainder of dividing a 4-bit number by 3. For example, if the input is 1010 the circuit produces a remainder output of 01 and if the input is 1111 the circuit produces an output of 00.

a. Derive the truth table of your circuit.

A ₁	A ₀	B ₁	B ₀	R ₁	R ₀
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	0	0

b. Using k-map simplification, find the minimum sum-of-products expressions for each of the output signals.

		B1 B0			
		00	01	11	10
A1 A0	00	0	1	0	0
	01	1	0	1	0
	11	0	1	0	0
	10	0	0	0	1

R₀

		B1 B0			
		00	01	11	10
A1 A0	00	0	0	0	1
	01	0	1	0	0
	11	0	0	0	1
	10	1	0	1	0

R₁

$$R_0 = A_1' A_0' B_1' B_0 + A_1' A_0 B_1 B_0 + A_1' A_0 B_1' B_0' + A_1 A_0 B_1' B_0 + A_1 A_0' B_1 B_0'$$

$$R_1 = A_1 A_0 B_1 B_0' + A_1' A_0' B_1 B_0' + A_1 A_0' B_1' B_0' + A_1 A_0' B_1 B_0 + A_1' A_0 B_1' B_0$$

c. Perform multilevel optimizations if possible.

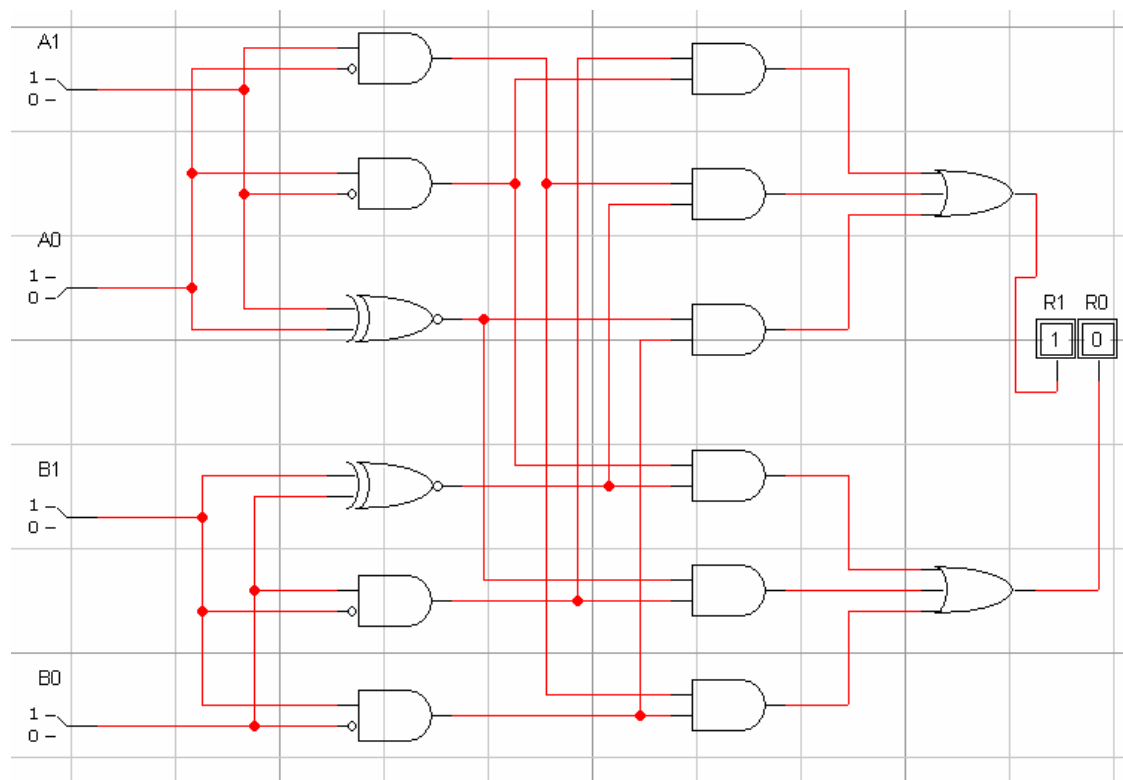
$$R_0 = A_1' A_0' B_1' B_0 + A_1' A_0 B_1 B_0 + A_1' A_0 B_1' B_0' + A_1 A_0 B_1' B_0 + A_1 A_0' B_1 B_0'$$

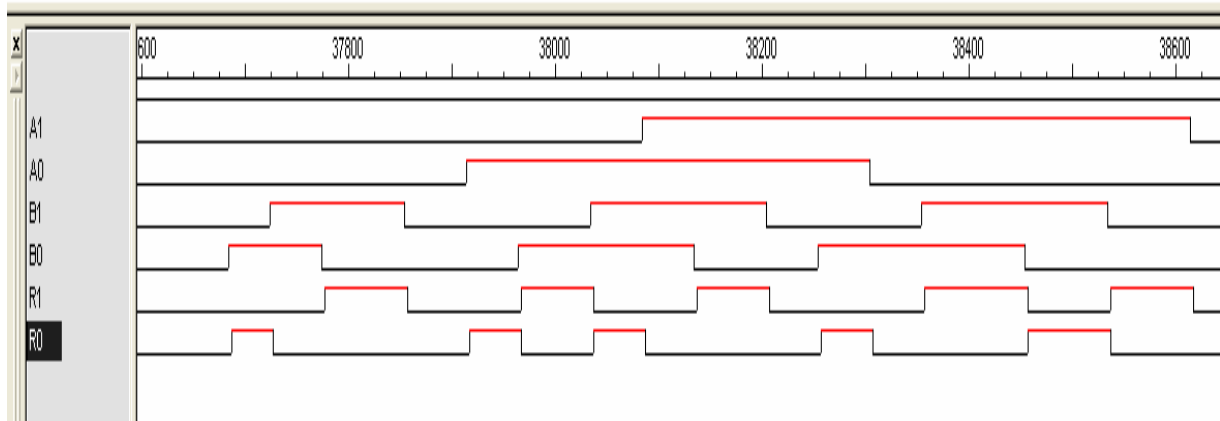
$$R_0 = A_1' A_0 (B_1 \oplus B_0) + B_1' B_0 (A_1 \oplus A_0) + A_1 A_0' B_1 B_0'$$

$$R_1 = A_1 A_0 B_1 B_0' + A_1' A_0' B_1 B_0' + A_1 A_0' B_1' B_0' + A_1 A_0' B_1 B_0 + A_1' A_0 B_1' B_0$$

$$R_1 = A_1 A_0' (B_1 \oplus B_0) + B_1 B_0' (A_1 \oplus A_0) + A_1' A_0 B_1' B_0$$

d. Model your circuit using logic works and verify that it is working properly by simulation. Provide a snapshot of your simulation waveform.





Q.2. (1% Bonus Question)

You are required to design a circuit that computes the remainder of dividing a N-bit number by 3., where N is a multiple of 4-bit numbers. The design needs to be modular in such a way that you design a cell that computes the remainder of dividing a 4-bit number by 3, and use this cell to construct the required circuit.

- a. Derive the truth table of your basic cell.

The circuit will be designed such that the remainder from the previous block is passed to the next block. This works as follows:

Suppose that you have an 8-bit number A_7-A_0 . Then the value of this number is $A_7 \times 2^7 + A_6 \times 2^6 + A_5 \times 2^5 + A_4 \times 2^4 + A_3 \times 2^3 + A_2 \times 2^2 + A_1 \times 2^1 + A_0 \times 2^0$.

The value of this number can be rewritten as $(A_7 \times 2^3 + A_6 \times 2^2 + A_5 \times 2^1 + A_4 \times 2^0) 2^4 + (A_3 \times 2^3 + A_2 \times 2^2 + A_1 \times 2^1 + A_0 \times 2^0)$.

Dividing the number $(A_3 \times 2^3 + A_2 \times 2^2 + A_1 \times 2^1 + A_0 \times 2^0)$ by 3 gives an answer = $[3 \times Q1 + R1]/3$.

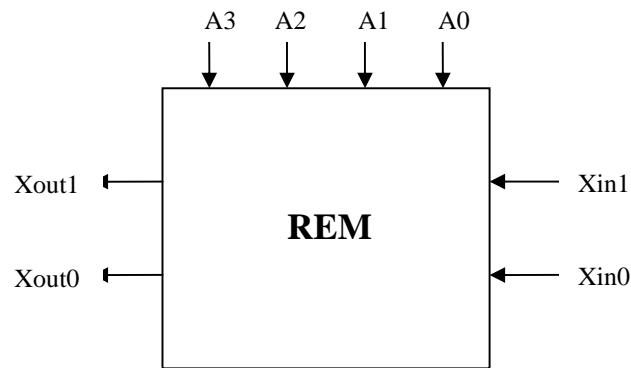
Dividing the number $(A_7 \times 2^3 + A_6 \times 2^2 + A_5 \times 2^1 + A_4 \times 2^0)$ by 3 gives an answer = $[3 \times Q2 + R2]/3$.

Dividing the number $(A_7 \times 2^3 + A_6 \times 2^2 + A_5 \times 2^1 + A_4 \times 2^0) 2^4$ by 3 gives an answer = $[3 \times Q2 \times 2^4 + (2^4 \times R2)]/3 = [3 \times Q2 \times 2^4 + 15 \times R2 + R2]/3$. Thus, this number will have a remainder of R2.

One can easily see now that the remainder of dividing the 8-bit number by 3 is the remainder of dividing $R1+R2$ by 3.

Thus, by feeding the remainder of the previous stage to the next stage, one can compute the whole number remainder.

So, the circuit will be designed as follows:



The truth table of the design is shown below:

A_3	A_2	A_1	A_0	R_1	R_0	X_{in1}	X_{in0}	X_{out1}	X_{out0}
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1	0
0	0	1	1	0	0	X	X	X	X
0	1	0	0	0	1	0	0	0	1
0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	0	1	0	0	0
0	1	1	1	0	1	X	X	X	X
1	0	0	0	1	0	0	0	1	0
1	0	0	1	0	0	0	1	0	0
1	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	X	X	X	X
1	1	0	0	0	0	X	X	X	X
1	1	0	1	0	1	X	X	X	X
1	1	1	0	1	0	X	X	X	X
1	1	1	1	0	0	X	X	X	X

Note that since the remainder of the circuit depends on the current remainder and the remainder from the previous number, we need only to design another circuit that produces X_{out1} and X_{out0} based on R_1 , R_0 , X_{in1} , and X_{in0} as shown below.

- b. Using k-map simplification, find the minimum sum-of-products expressions for each of the output signals.

		X _{in1} X _{in0}			
		00	01	11	10
R ₁ R ₀	00	0	0	X	1
	01	0	1	X	0
	11	X	X	X	X
	10	1	0	X	0

X_{out1}

		X _{in1} X _{in0}			
		00	01	11	10
R ₁ R ₀	00	0	1	X	0
	01	1	0	X	0
	11	X	X	X	X
	10	0	0	X	1

X_{out0}

$$X_{out0} = R_1 X_{in1} + R_0 X_{in1}' X_{in0}' + R_1' R_0' X_{in0}$$

$$X_{out1} = R_0 X_{in0} + R_1 X_{in1}' X_{in0}' + R_1' R_0' X_{in1}$$

- c. Perform multilevel optimizations if possible.

Optimizations are possible by sharing the AND gate for computing $X_{in1}' X_{in0}'$ and the AND gate for computing $R_1' R_0'$.

- d. Model your cell using logic works and verify that it is working properly by simulation. Provide a snapshot of your simulation waveform.

- e. Using your design cell, construct a circuit that computes the remainder of dividing an 8-bit number by 3. Verify the correct functionality of your circuit by simulation.

