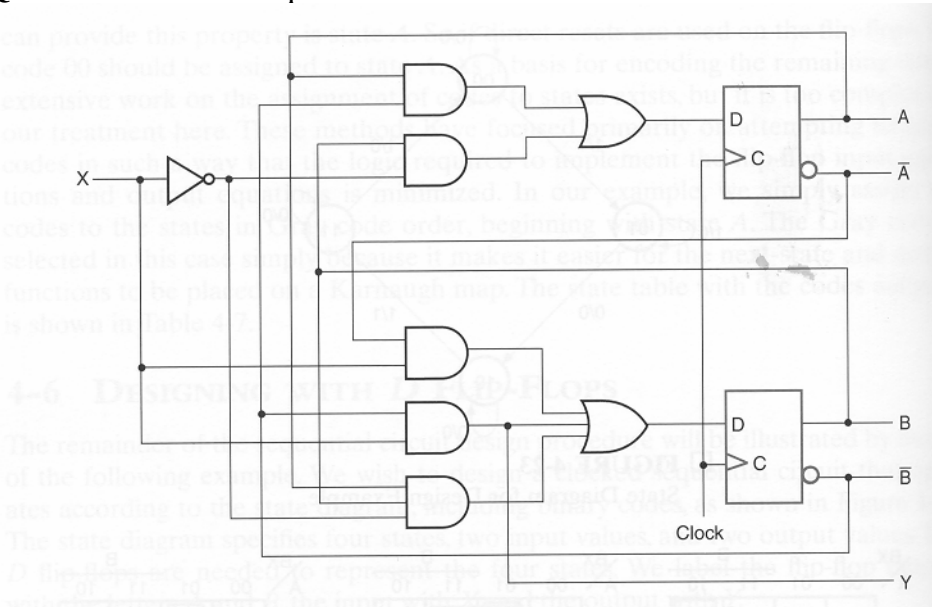


**COE 202, Term 052**  
**Fundamentals of Computer Engineering**  
**HW# 6**

**Q.1.** Consider the sequential circuit shown below:



- (i) Starting from the state 00, determine the state transitions and output sequence that will be generated when the input sequence 11001101 is applied.
  - (ii) Determine the maximum clock frequency under which the circuit will operate correctly given that the propagation delay of the inverter gate is 2ns, the AND gate is 4ns, and the OR gate is 4ns. Assume that the D-FF has a setup time of 2ns, a hold time of 1ns, and a propagation delay of 2ns.
- Q.2.** A set-dominant flip-flop has set and reset inputs. It differs from a conventional SR flip-flop in that, when both S and R are equal to 1, the flip-flop is set.
- (i) Obtain the characteristic table of the set-dominant flip-flop.
  - (ii) Derive the excitation table for the set-dominant flip-flop.
  - (iii) Design a positive-edge triggered set-dominant flip-flop using D-FF.
  - (iv) Design a positive-edge triggered set-dominant flip-flop using JK-FF.

**Q.3.** Design a sequential circuit with two flip-flops A and B and two inputs E and X. If E=0, the circuit remains in the same state, regardless of the value of X. When E=1 and X=1, the circuit goes through the state transitions from 00 to 01 to 10 to 11, back to 00, and then repeats. When E=1 and X=0, the circuit goes through the state transitions from 00 to 11 to 10 to 01, back to 00, and then repeats. Design the circuit using the following types of FFs:

- (i) Positive-edge-triggered D-FF.
- (ii) Positive-edge-triggered JK-FF.
- (iii) Positive-edge-triggered T-FF.

**Q.4.** A single-input, single-output sequential circuit is to be designed that recognizes only the two input sequences 0110 and 1111 applied to its inputs any time they occur in the input stream. If any of these two sequences is detected the output will be 1, otherwise it will be 0.

- (i) Show the state diagram for this circuit assuming no detection of overlapping sequences.
- (ii) Show the state diagram for this circuit assuming detection of overlapping sequences.

**Q.5.** You are to design a serial adder A3 that computes the sum of three separate serial input streams rather than the usual two. The adder has three primary inputs  $X_1$ ,  $X_2$ ,  $X_3$ , and a single primary output Z. Using D flip-flops and any standard gates, construct the state table, excitation table, and a logic circuit diagram for A3.

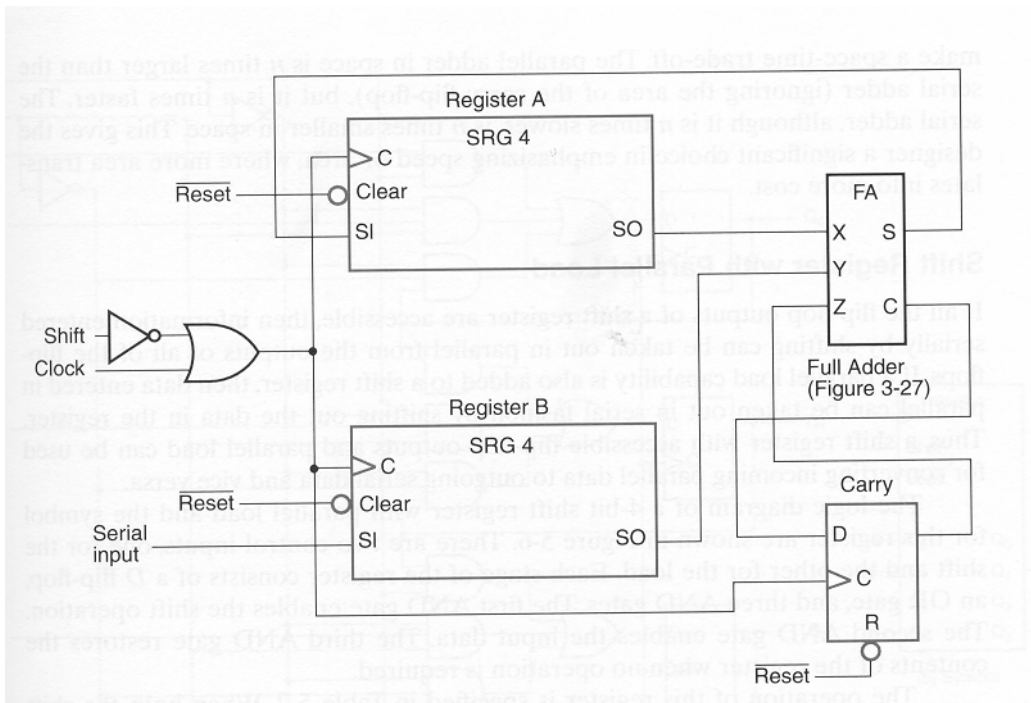
**Q.6.** Minimize the state table shown below and determine the reduced state table:

| Current State | Next State |     | Output |     |
|---------------|------------|-----|--------|-----|
|               | X=0        | X=1 | X=0    | X=1 |
| A             | F          | B   | 0      | 0   |
| B             | D          | C   | 0      | 0   |
| C             | F          | E   | 0      | 0   |
| D             | G          | A   | 1      | 0   |
| E             | D          | C   | 0      | 0   |
| F             | F          | B   | 1      | 1   |
| G             | G          | H   | 0      | 1   |
| H             | G          | A   | 1      | 0   |

**Q.7.** A sequential circuit MON is to be designed that monitors the condition of a patient in a hospital bed. The input to MON is a binary number n that ranges in value from 1 to 7 and indicates the patient's condition. The expected value of n is sent to MON automatically every five seconds. If n

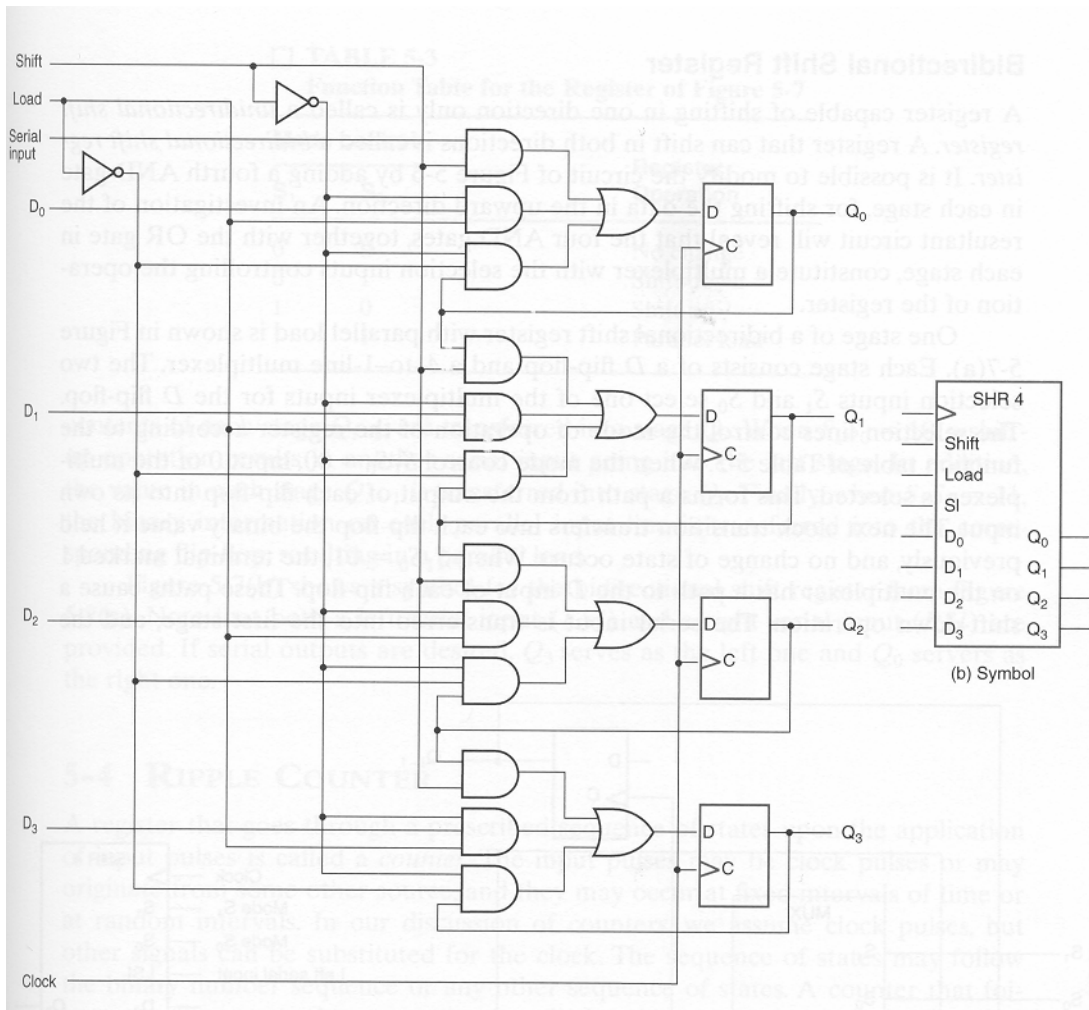
goes below 2 or above 4 on two or more occasions, the machine should activate an alarm at a nurse's station. The nurse responds by administering medication to the patient and resetting the monitor. Using JK flip-flops and NOR gates only, carry out the logic design of MON. Obtain a state table, a state assignment, and a complete logic diagram.

**Q.8.** What changes are needed in the figure shown below to convert it to a serial subtractor that subtracts the contents of register B from the contents of register A. Explain how it is possible to detect whether  $A < B$ . If  $A < B$ , what will be the relationship of the result of the subtraction to the correct result?



**Q.9.** Modify the register shown below so that it will operate according to the following function table using selection inputs  $s_1$  and  $s_0$ .

| $s_1$ | $s_0$ | Register Operation  |
|-------|-------|---------------------|
| 0     | 0     | No change           |
| 0     | 1     | Clear register to 0 |
| 1     | 0     | Shift down          |
| 1     | 1     | Load parallel data  |



- Q.10.** A negative edge-triggered flip-flop has a 4-ns delay between the time its C input goes from 1 to 0 and the time the output is complemented. What is the maximum delay in a 12-bit binary ripple counter that uses these flip-flops? What is the maximum frequency at which the counter can operate reliably?
- Q.11.** Draw the logic diagram of a 4-bit ripple binary down-counter using:
- (i) Flip-flops that trigger on the positive transition of the clock.
  - (ii) Flip-flops that trigger on the negative transition of the clock.
- Q.12.** Construct a 12-bit serial-parallel counter, using three 4-bit parallel counters. What is the maximum number of AND gates in a chain that a signal must propagate through in the 12-bit counter.

HW#6

Q1 (i)

$$00 \xrightarrow[\gamma=1]{x=1} 01 \xrightarrow[\gamma=0]{x=1} 01 \xrightarrow[\gamma=0]{x=0} 10 \xrightarrow[\gamma=0]{x=0} 10$$

$$10 \xrightarrow[\gamma=1]{x=1} 11 \xrightarrow[\gamma=0]{x=1} 00 \xrightarrow[\gamma=0]{x=0} 00 \xrightarrow[\gamma=1]{x=1} 01$$

(ii) For the circuit to operate correctly, the clock period  $T$  has to satisfy the following constraint:

$$T > t_{ff}^{\max} + t_c^{\max} + t_{su}^{\max}$$

$$t_{ff}^{\max} = 2 \text{ ns}$$

$$t_c^{\max} = \max(t_{c1}, t_{c2})$$

$$t_{c1} = 4 \text{ ns}$$

$$t_{c2} = 2 \text{ ns} + 4 \text{ ns} + 4 \text{ ns} = 10 \text{ ns}$$

$$t_c^{\max} = 10 \text{ ns}$$

$$t_{su}^{\max} = 2 \text{ ns}$$

$$\text{Thus, } T > 2 \text{ ns} + 10 \text{ ns} + 2 \text{ ns} = 14 \text{ ns}$$

$$\text{The maximum frequency } f = \frac{1}{T} < \frac{1}{14 \text{ ns}} = 71.4 \text{ MHz}$$

If we add a 10% safety margin, then  $T = 15.4 \text{ ns}$

$$\text{and } f = 65 \text{ MHz}$$

$$\text{Note } t_h^{\min} = 2 \text{ ns} < t_{ff}^{\min} + t_c^{\min} = 2 \text{ ns} + 8 \text{ ns} = 10 \text{ ns}$$

So, the hold time constraint is satisfied.

Q2 Set-dominant flip-flop

(i) Characteristic table

| S | R | Q(t+1) |
|---|---|--------|
| 0 | 0 | Q(t)   |
| 0 | 1 | 0      |
| 1 | 0 | 1      |
| 1 | 1 | 1      |

(ii) Excitation table

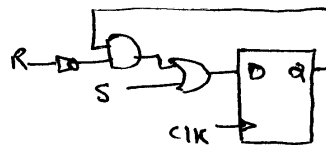
| Q(t) | Q(t+1) | S | R        |
|------|--------|---|----------|
| 0    | 0      | 0 | X        |
| 0    | 1      | 1 | X        |
| 1    | 0      | 0 | 1        |
| 1    | 1      | X | 0 or 1 X |

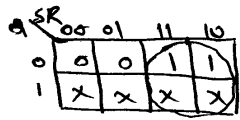
(iii)  
(iv)

| Q(t) | S | R | Q(t+1) | D | J | K |
|------|---|---|--------|---|---|---|
| 0    | 0 | 0 | 0      | 0 | 0 | X |
| 0    | 0 | 1 | 0      | 0 | 0 | X |
| 0    | 1 | 0 | 1      | 1 | 1 | X |
| 0    | 1 | 1 | 1      | 1 | 1 | X |
| 1    | 0 | 0 | 1      | 1 | X | 0 |
| 1    | 0 | 1 | 0      | 0 | X | 0 |
| 1    | 1 | 0 | 1      | 1 | X | 0 |
| 1    | 1 | 1 | 1      | 1 | X | 0 |

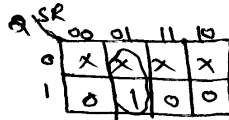
| SR | 00 | 01 | 11 | 10 |
|----|----|----|----|----|
| 0  | 0  | 0  | 1  | 1  |
| 1  | 1  | 0  | 1  | 1  |

$$D = S + Q\bar{R}$$

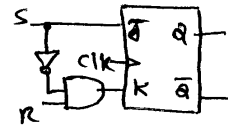




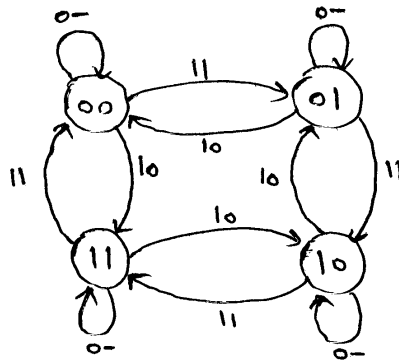
$J = S$



$K = \bar{S}R$



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State Diagram

- State table:

| current state |   | next state |       |       |       |
|---------------|---|------------|-------|-------|-------|
| A             | B | EX=00      | EX=01 | EX=10 | EX=11 |
| 0             | 0 | 00         | 00    | 11    | 01    |
| 0             | 1 | 01         | 01    | 00    | 10    |
| 1             | 0 | 10         | 10    | 01    | 11    |
| 1             | 1 | 11         | 11    | 10    | 00    |

(i) Design with positive-edge-triggered D-FF

|         |    |    |    |    |
|---------|----|----|----|----|
| AB \ EX | 00 | 01 | 11 | 10 |
| 00      | 0  | 0  | 0  | 1  |
| 01      | 0  | 0  | 1  | 0  |
| 11      | 1  | 1  | 0  | 1  |
| 10      | 1  | 1  | 1  | 0  |

|   |   |   |   |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |

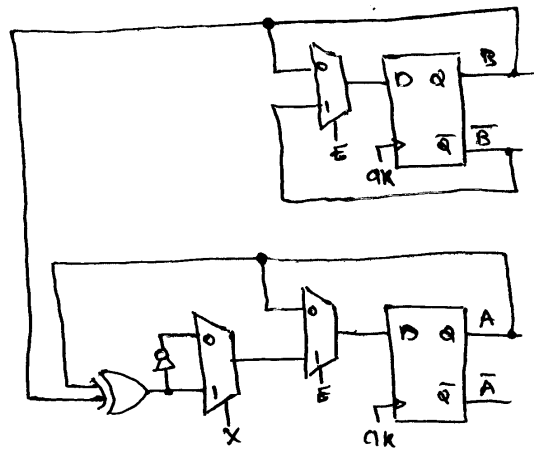
$$D_A = A\bar{E} + A\bar{B}X + AB\bar{X} + \bar{A}BEX + \bar{A}\bar{B}E\bar{X}$$

$$D_B = B\bar{E} + \bar{B}E$$

OR

$$D_A = A\bar{E} + XEA\bar{B} + AB\bar{X}E + \bar{A}BEX + \bar{A}\bar{B}E\bar{X}$$

$$= A\bar{E} + E[\bar{X}[AB + \bar{A}\bar{B}] + X[A\bar{B} + \bar{A}B]]$$





(ii) Design with positive-edge-triggered JK FF

|         |    |    |    |    |
|---------|----|----|----|----|
| AB \ EX | 00 | 01 | 11 | 10 |
| 00      | 0  | 0  | 0  | 1  |
| 01      | 0  | 0  | 1  | 0  |
| 11      | X  | X  | X  | X  |
| 10      | X  | X  | X  | X  |

$$J_A = BEX + \bar{B}E\bar{X}$$

|         |    |    |    |    |
|---------|----|----|----|----|
| AB \ EX | 00 | 01 | 11 | 10 |
| 00      | X  | X  | X  | X  |
| 01      | X  | X  | X  | X  |
| 11      | 0  | 0  | 1  | 0  |
| 10      | 0  | 0  | 0  | 1  |

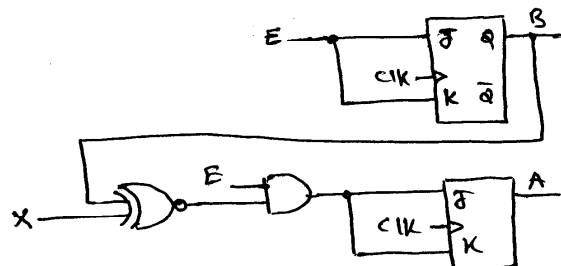
$$K_A = J_A = BEX + \bar{B}E\bar{X}$$

|         |    |    |    |    |
|---------|----|----|----|----|
| AB \ EX | 00 | 01 | 11 | 10 |
| 00      | 0  | 0  | 1  | 1  |
| 01      | X  | X  | X  | X  |
| 11      | 0  | 0  | 1  | 1  |
| 10      | X  | X  | X  | X  |

$$J_B = E$$

|         |    |    |    |    |
|---------|----|----|----|----|
| AB \ EX | 00 | 01 | 11 | 10 |
| 00      | X  | X  | X  | X  |
| 01      | 0  | 0  | 1  | 1  |
| 11      | X  | X  | X  | X  |
| 10      | 0  | 0  | 1  | 1  |

$$K_B = E$$



(iii) Design with positive-edge-triggered T FF

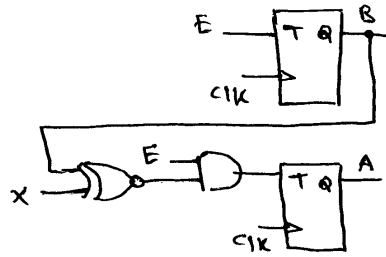
|         |    |    |    |    |
|---------|----|----|----|----|
| AB \ EX | 00 | 01 | 11 | 10 |
| 00      | 0  | 0  | 0  | 1  |
| 01      | 0  | 0  | 1  | 0  |
| 11      | 0  | 0  | 1  | 0  |
| 10      | 0  | 0  | 0  | 1  |

$$T_A = BEX + \bar{B}E\bar{X}$$

$$= E(B \oplus X)'$$

|         |    |    |    |    |
|---------|----|----|----|----|
| AB \ EX | 00 | 01 | 11 | 10 |
| 00      | 0  | 0  | 1  | 1  |
| 01      | 0  | 0  | 1  | 1  |
| 11      | 0  | 0  | 1  | 1  |
| 10      | 0  | 0  | 1  | 1  |

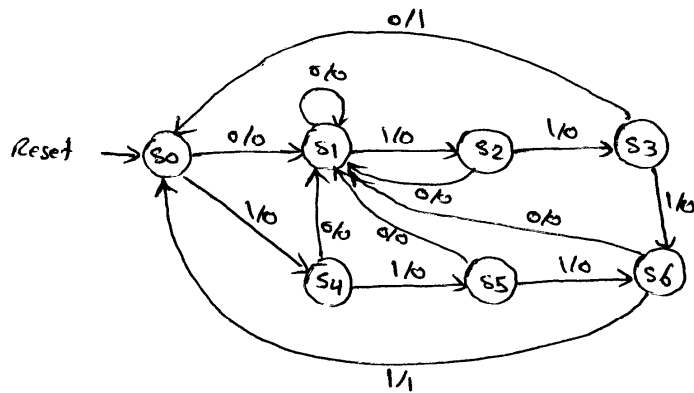
$$T_B = E$$



Note that the design of the circuit with T-FF could have been obtained directly from the JK-FF since a JK-FF with the J and K inputs connected together produces a T-FF.

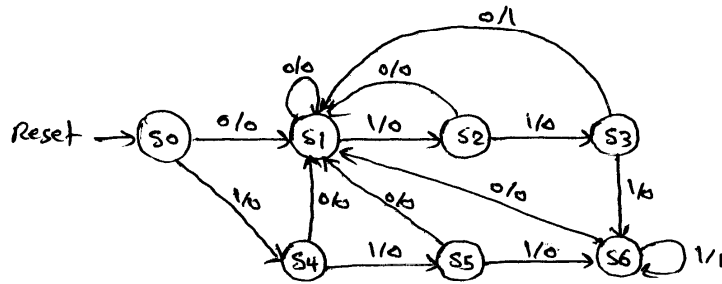
Q4

(i) State diagram with no overlapping:



Note that it is assumed here that state  $S_0$  is the reset state, i.e. when the Reset input is high the machine will start from state  $S_0$ .

(ii) state diagram with overlapping:



Q5 Note that in the design of a 3-input serial adder, it is not sufficient to use a single bit for holding the carry out of addition. It is necessary to use two bits to represent the carry out as its value is greater than 1.

state table:

| current state |    | input |    |    | Next state |    | output |
|---------------|----|-------|----|----|------------|----|--------|
| C1            | C0 | X1    | X2 | X3 | C1         | C0 | Z      |
| 0             | 0  | 0     | 0  | 0  | 0          | 0  | 0      |
| 0             | 0  | 0     | 0  | 1  | 0          | 0  | 1      |
| 0             | 0  | 0     | 1  | 0  | 0          | 0  | 1      |
| 0             | 0  | 0     | 1  | 1  | 0          | 1  | 0      |
| 0             | 0  | 1     | 0  | 0  | 0          | 0  | 1      |
| 0             | 0  | 1     | 0  | 1  | 0          | 1  | 0      |
| 0             | 0  | 1     | 1  | 0  | 0          | 1  | 0      |
| 0             | 0  | 1     | 1  | 1  | 0          | 1  | 1      |
| 0             | 1  | 0     | 0  | 0  | 0          | 0  | 1      |
| 0             | 1  | 0     | 0  | 1  | 0          | 1  | 0      |
| 0             | 1  | 0     | 1  | 0  | 0          | 1  | 0      |
| 0             | 1  | 0     | 1  | 1  | 0          | 1  | 1      |
| 0             | 1  | 1     | 0  | 0  | 0          | 1  | 0      |
| 0             | 1  | 1     | 0  | 1  | 0          | 1  | 1      |
| 0             | 1  | 1     | 1  | 0  | 1          | 0  | 0      |
| 1             | 0  | 0     | 0  | 0  | 0          | 1  | 0      |
| 1             | 0  | 0     | 0  | 1  | 0          | 1  | 1      |
| 1             | 0  | 0     | 1  | 0  | 0          | 1  | 1      |
| 1             | 0  | 0     | 1  | 1  | 1          | 0  | 0      |
| 1             | 0  | 1     | 0  | 0  | 0          | 1  | 1      |
| 1             | 0  | 1     | 0  | 1  | 1          | 0  | 0      |
| 1             | 0  | 1     | 1  | 0  | 1          | 0  | 0      |
| 1             | 0  | 1     | 1  | 1  | 1          | 0  | 1      |

$c_1 = 0$

|                   |    |    |    |    |
|-------------------|----|----|----|----|
| $c_0 x_1 x_2 x_3$ | 00 | 01 | 11 | 10 |
| 00                | 0  | 1  | 0  | 1  |
| 01                | 1  | 0  | 1  | 0  |
| 11                | 0  | 1  | 0  | 1  |
| 10                | 1  | 0  | 1  | 0  |

$c_1 = 1$

|   |   |   |   |
|---|---|---|---|
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| x | x | x | x |
| x | x | x | x |

$$Z = c_0 \oplus x_1 \oplus x_2 \oplus x_3$$

$c_1 = 0$

|                   |    |    |    |    |
|-------------------|----|----|----|----|
| $c_0 x_1 x_2 x_3$ | 00 | 01 | 11 | 10 |
| 00                | 0  | 0  | 0  | 0  |
| 01                | 0  | 0  | 0  | 0  |
| 11                | 0  | 0  | 1  | 0  |
| 10                | 0  | 0  | 0  | 0  |

$c_1 = 1$

|   |   |   |   |
|---|---|---|---|
| 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 |
| x | x | x | x |
| x | x | x | x |

$$D_1 = c_1 x_1 (x_2 + x_3) + c_0 x_1 x_2 x_3 + c_1 x_2 x_3$$

$c_1 = 0$

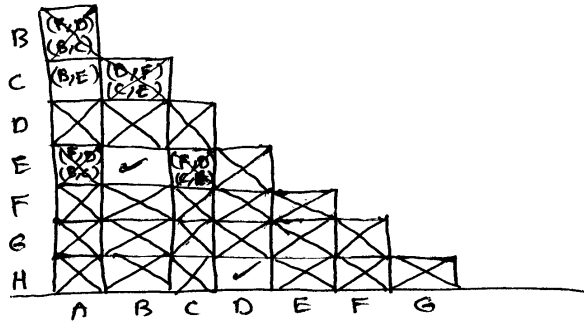
|                   |    |    |    |    |
|-------------------|----|----|----|----|
| $c_0 x_1 x_2 x_3$ | 00 | 01 | 11 | 10 |
| 00                | 0  | 0  | 0  | 0  |
| 01                | 0  | 0  | 0  | 0  |
| 11                | 0  | 0  | 0  | 0  |
| 10                | 0  | 0  | 0  | 0  |

$c_1 = 1$

|   |   |   |   |
|---|---|---|---|
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| x | x | x | x |
| x | x | x | x |

$$D_0 = c_0 \bar{x}_2 x_3 + c_0 x_2 \bar{x}_3 + c_0 x_1 \bar{x}_2 + \bar{x}_1 x_2 x_3 \bar{c}_1 + \bar{c}_1 \bar{c}_0 x_1 x_2 + \bar{c}_1 \bar{c}_0 x_1 x_3 + c_1 \bar{x}_1 \bar{x}_2 + c_1 \bar{x}_1 \bar{x}_3$$

Q6



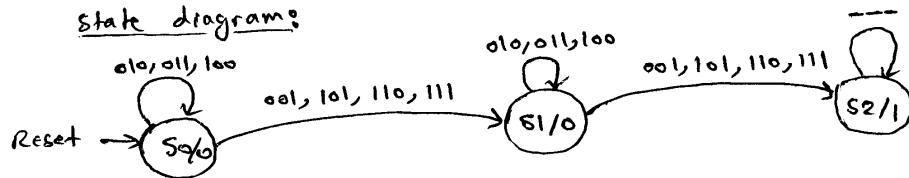
So, from the implication chart, we see that the states (A,C), (B,E), and (D,H) are equivalent.

The reduced state table:

| Current state | Next state |     | Output |     |
|---------------|------------|-----|--------|-----|
|               | x=0        | x=1 | x=0    | x=1 |
| A             | F          | B   | 0      | 0   |
| B             | D          | A   | 0      | 0   |
| D             | G          | A   | 1      | 0   |
| F             | F          | B   | 1      | 1   |
| G             | G          | D   | 0      | 1   |

Q7

State diagram:



State table:

| Current state | x | y | z | Next state | output |
|---------------|---|---|---|------------|--------|
| S0            | 0 | 0 | 0 | -          | 0      |
| S0            | 0 | 0 | 1 | S1         | 0      |
| S0            | 0 | 1 | 0 | S0         | 0      |
| S0            | 0 | 1 | 1 | S0         | 0      |
| S0            | 1 | 0 | 0 | S0         | 0      |
| S0            | 1 | 0 | 1 | S1         | 0      |
| S0            | 1 | 1 | 0 | S1         | 0      |
| S0            | 1 | 1 | 1 | S1         | 0      |
| S0            | 0 | 0 | 0 | -          | 0      |
| S1            | 0 | 0 | 1 | S2         | 0      |
| S1            | 0 | 1 | 0 | S1         | 0      |
| S1            | 0 | 1 | 1 | S1         | 0      |
| S1            | 1 | 0 | 0 | S1         | 0      |
| S1            | 1 | 0 | 1 | S2         | 0      |
| S1            | 1 | 1 | 0 | S2         | 0      |
| S1            | 1 | 1 | 1 | S2         | 0      |
| S1            | - | - | - | S2         | 1      |
| S2            | - | - | - | -          | -      |

We choose the following state assignment:

$$S_0 = 00, S_1 = 01, S_2 = 11$$

So, we need two JK FFs since we have three states.

$x=0$

|           |      |    |    |    |    |
|-----------|------|----|----|----|----|
| $q_1 q_0$ | $yz$ | 00 | 01 | 11 | 10 |
| 00        | X    | 0  | 0  | 0  | 0  |
| 01        | X    | 1  | 0  | 0  | 0  |
| 11        | X    | X  | X  | X  | X  |
| 10        | X    | X  | X  | X  | X  |

$x=1$

|   |   |   |   |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| X | X | X | X |
| X | X | X | X |

$$\begin{aligned} \bar{J}_{q_1} &= x q_0 y \\ &+ q_0 \bar{y} z \\ &= q_0 (xy + \bar{y}z) \end{aligned}$$

$x=0$

|           |       |    |    |    |    |
|-----------|-------|----|----|----|----|
| $q_1 q_0$ | $y z$ | 00 | 01 | 11 | 10 |
| 00        | X     | X  | X  | X  | X  |
| 01        | X     | X  | X  | X  | X  |
| 11        | 0     | 0  | 0  | 0  |    |
| 10        | X     | X  | X  | X  |    |

$x=1$

|   |   |   |   |
|---|---|---|---|
| X | X | X | X |
| X | X | X | X |
| 0 | 0 | 0 | 0 |
| X | X | X | X |

$$K_{q_1} = 0$$

$x=0$

|           |       |    |    |    |    |
|-----------|-------|----|----|----|----|
| $q_1 q_0$ | $y z$ | 00 | 01 | 11 | 10 |
| 00        | X     | 1  | 0  | 0  |    |
| 01        | X     | X  | X  | X  |    |
| 11        | X     | X  | X  | X  |    |
| 10        | X     | X  | X  | X  |    |

$x=1$

|   |   |   |   |
|---|---|---|---|
| 0 | 1 | 1 | 1 |
| X | X | X | X |
| X | X | X | X |
| X | X | X | X |

$$\bar{D}_{q_0} = xy + \bar{y}z$$

$x=0$

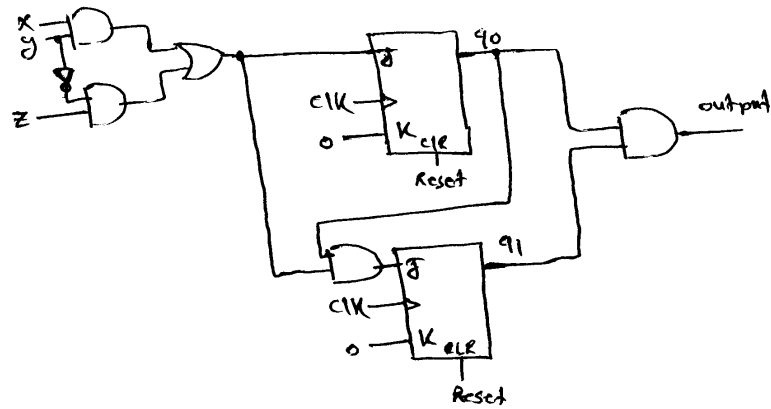
|           |       |    |    |    |    |
|-----------|-------|----|----|----|----|
| $q_1 q_0$ | $y z$ | 00 | 01 | 11 | 10 |
| 00        | X     | X  | X  | X  |    |
| 01        | X     | 0  | 0  | 0  |    |
| 11        | 0     | 0  | 0  | 0  |    |
| 10        | X     | X  | X  | X  |    |

$x=1$

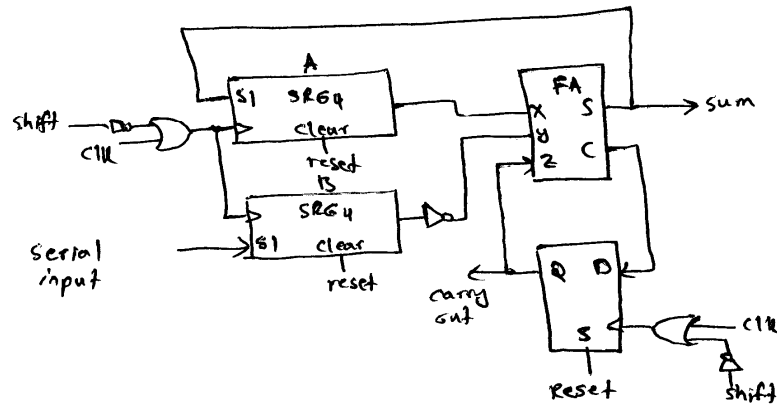
|   |   |   |   |
|---|---|---|---|
| X | X | X | X |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 |
| X | X | X | X |

$$K_{q_0} = 0$$

output =  $q_1 q_0$



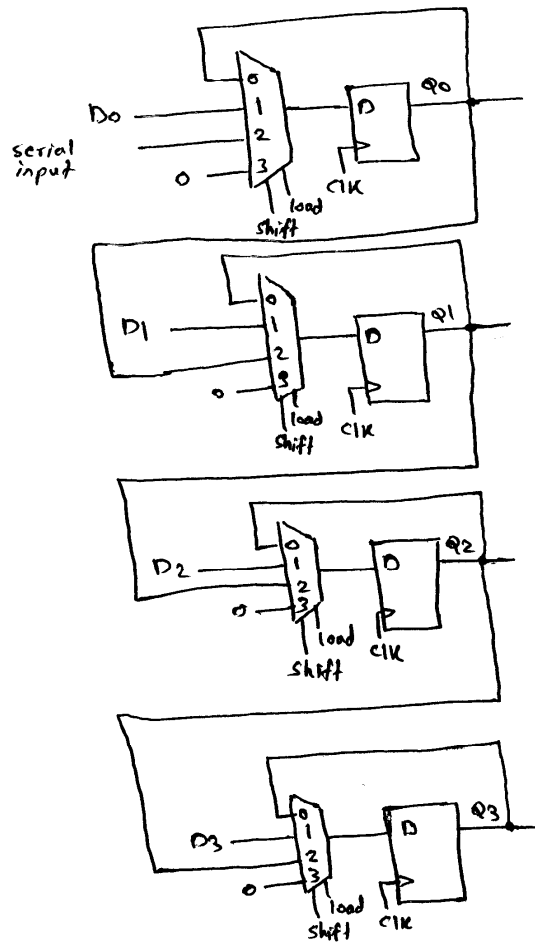
Q8 Figure 5-5 i.e. the serial adder can be converted to a serial subtractor as follows :



Note that when Reset is set to high, the FF will be set to high i.e. the carry value will be 1.

Thus,  $A + \bar{B} + 1 = A - B$ . Note that to first shift a number in register A, we have to shift its 2's complement. If  $A < B$ , the carry out will be 0.

Q9



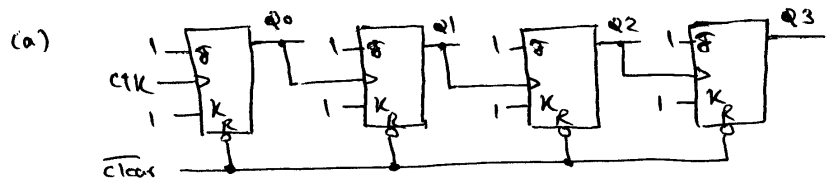
Q10

The maximum delay in a 12-bit binary ripple counter =  $12 * 4ns = 48ns$

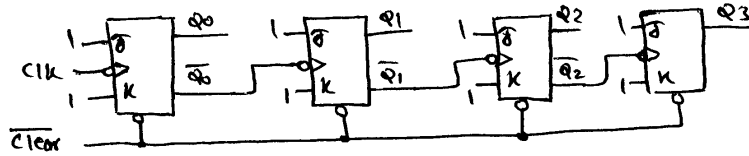
The maximum frequency at which the counter can operate reliably is  $f = \frac{1}{48ns} = 20.8 MHz$



Q11

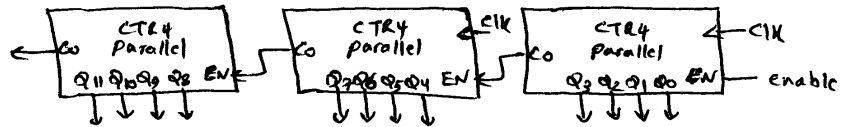


(b)



Q12

12-bit serial-parallel counter



The maximum number of AND gates in a chain that a signal must propagate through in the 12-bit counter is 3.