Q.1. Consider the sequential circuit shown below:
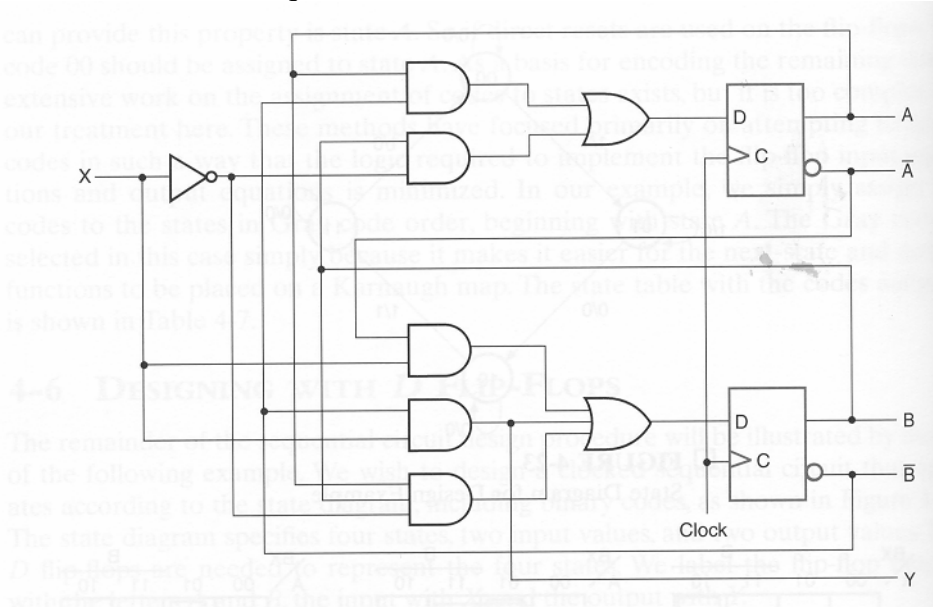
(i) Starting from the state 00, determine the state transitions and output sequence that will be generated when the input sequence 11001101 is applied.

(ii) Determine the maximum clock frequency under which the circuit will operate correctly given that the propagation delay of the inverter gate is 2ns, the AND gate is 4ns, and the OR gate is 4ns. Assume that the D-FF has a setup time of 2ns, a hold time of 1ns, and a propagation delay of 2ns.

Q.2. A set-dominant flip-flop has set and reset inputs. It differs from a conventional SR flip-flop in that, when both S and R are equal to 1, the flip-flop is set.

(i) Obtain the characteristic table of the set-dominant flip-flop.

(ii) Derive the excitation table for the set-dominant flip-flop.

(iii) Design a positive-edge triggered set-dominant flip-flop using D-FF.

(iv) Design a positive-edge triggered set-dominant flip-flop using JK-FF.

Q.3. Design a sequential circuit with two flip-flops A and B and two inputs E and X. If E=0, the circuit remains in the same state, regardless of the value of X. When E=1 and X=1, the circuit goes through the state transitions from 00 to 01 to 10 to 11, back to 00, and then repeats. When E=1 and X=0, the circuit goes through the

state transitions from 00 to 11 to 10 to 01, back to 00, and then repeats. Design the circuit using the following types of FFs:

(i) Positive-edge-triggered D-FF.

(ii) Positive-edge-triggered JK-FF.

(iii) Positive-edge-triggered T-FF.

Q.4. A single-input, single-output sequential circuit is to be designed that recognizes only the two input sequences 0110 and 1111 applied to its inputs any time they occur in the input stream. If any of these two sequences is detected the output will be 1, otherwise it will be 0.

(i) Show the state diagram for this circuit assuming no detection of overlapping sequences.

(ii) Show the state diagram for this circuit assuming detection of overlapping sequences.

Q.5. You are to design a serial adder A3 that computes the sum of three separate serial input streams rather than the usual two. The adder has three primary inputs X_1, X_2, X_3, and a single primary output Z. Using D flip-flops and any standard gates, construct the state table, excitation table, and a logic circuit diagram fro A3.

**Q.6.** Minimize the state table shown below and determine the reduced state table:

Current State	Next State		Output	
	X=0	X=1	X=0	X=1
A	F	B	0	0
B	D	C	0	0
C	F	E	0	0
D	G	A	1	0
E	D	C	0	0
F	F	B	1	1
G	G	H	0	1
H	G	A	1	0

Q.7. A sequential circuit MON is to be designed that monitors the condition of a patient in a hospital bed. The input to MON is a binary number n that ranges in value from 1 to 7 and indicates the patient`s condition. The expected value of n is sent to MON automatically every five seconds. If n goes below 2 or above 4 on two or more occasions, the machine should activate an alarm at a nurse`s station. The nurse responds by administering medication to the patient and resetting the monitor. Using JK flip-flops and NOR gates only, carry out the logic design of MON. Obtain a state table, a state assignment, and a complete logic diagram.

Q.8. What changes are needed in the figure shown below to convert it to a serial subtractor that subtracts the contents of register B from the contents of register A. Explain how it is possible to detect whether A < B. If A < B, what will be the relationship of the result of the subtraction to the correct result?
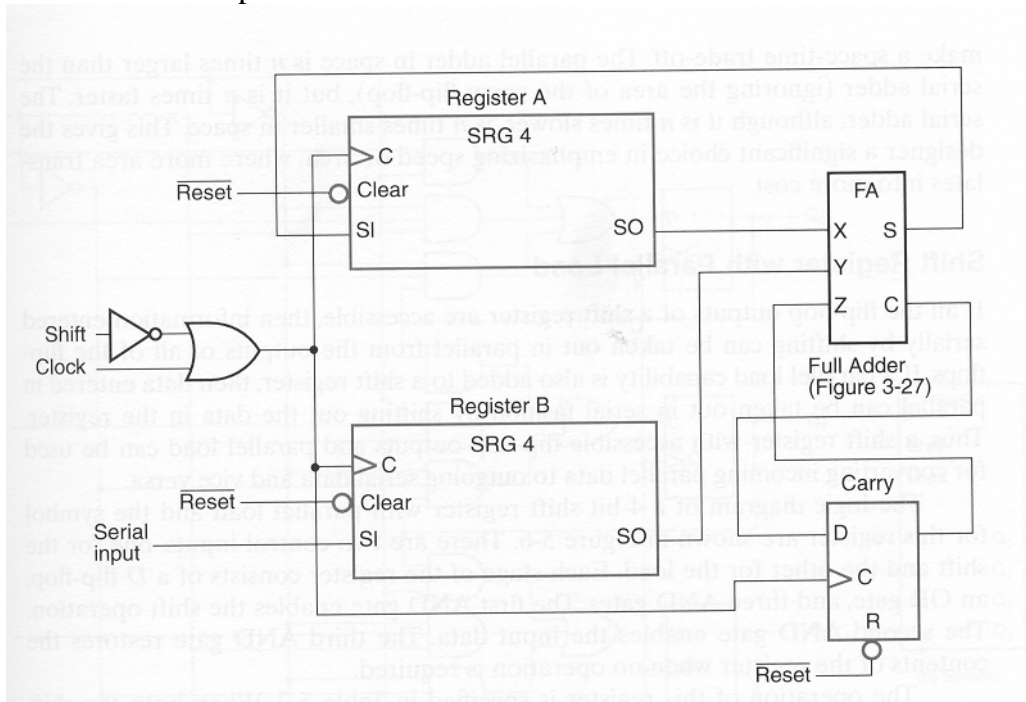
Q.9. Modify the register shown below so that it will operate according to the following function table using selection inputs s_1 and s_0.

S_1	S_0	Register Operation
0	0	No change
0	1	Clear register to 0
1	0	Shift down
1	1	Load parallel data

(b) Symbol
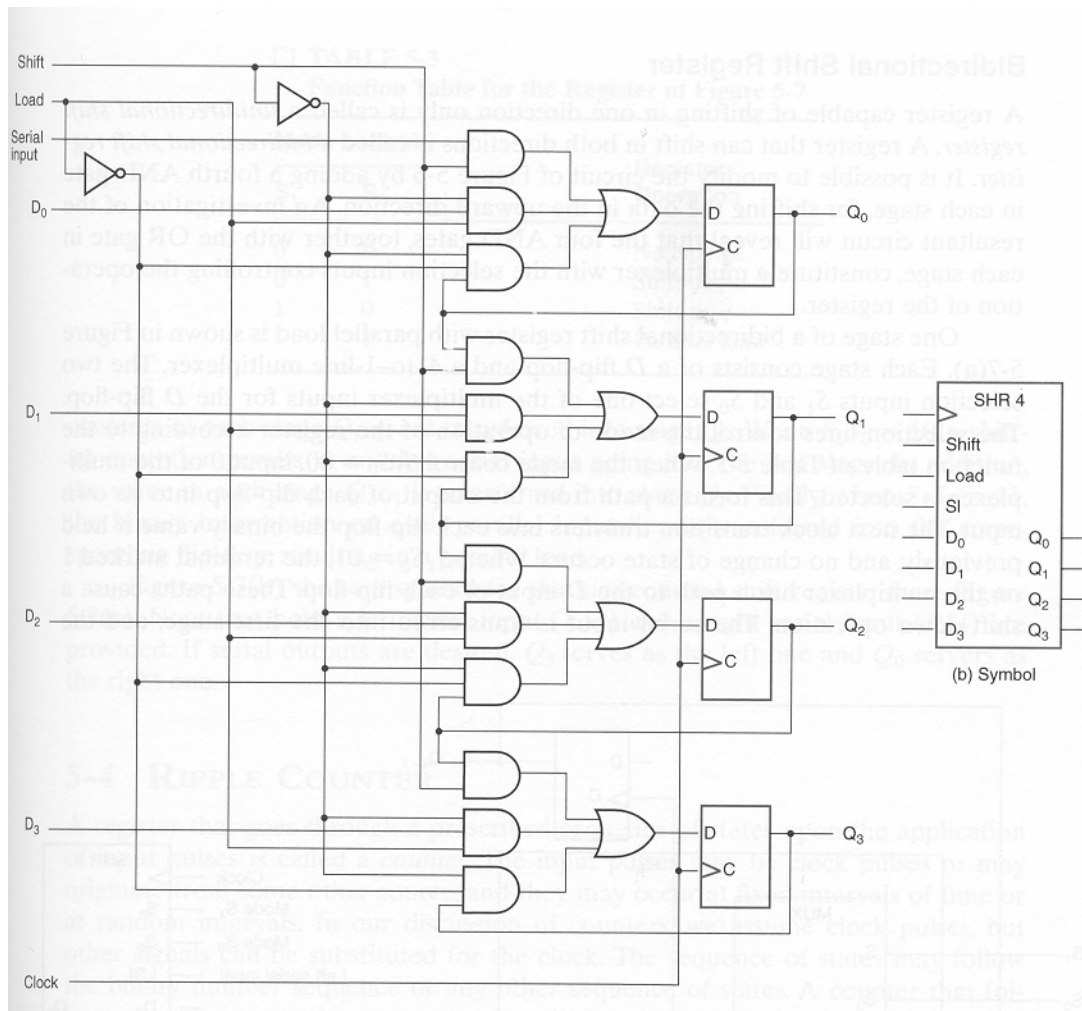
Q.10. A negative edge-triggered flip-flop has a 4-ns delay between the time its C input goes from 1 to 0 and the time the output is complemented. What is the maximum delay in a 12-bit binary ripple counter that uses these flip-flops? What is the maximum frequency at which the counter can operate reliably?

Q.11. Draw the logic diagram of a 4-bit ripple binary down-counter using:

(i)   Flip-flops that trigger on the positive transition of the clock.

(ii) Flip-flops that trigger on the negative transition of the clock.

Q.12. Construct a 12-bit serial-parallel counter, using three 4-bit parallel counters. What is the maximum number of AND gates in a chain that a signal must propagate through in the 12-bit counter.